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EVALUATION OF THE NANOSCALE TECHNOLOGY USING FINFET BASED SRAM CELL DESIGN

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ABSTRACT:-

The static power variation, SNM, RNM, and WNM for a nanoscale FinFET-based SRAM cell with regard to driver, load, and breadth of access are analyzed in this work. Semiconductor devices may now be greatly reduced to the nanoscale thanks to FinFET technology. This is due to the fact that the improved control of the FinFET device structure produces a much lower leakage current, which results in a relatively high Ion/ Ioff ratio.

In addition, the effect of process variation on the SRAM cell's performance was investigated by a Monte Carlo simulation with HSPICE. FinFET-based SRAM cells may be implemented at sub-10nm scales, which makes them appropriate for advanced integrated circuits, depending on the particular process technology and node. The simulation was ran for 1000 values, assuming that 3srepresents 10% of the mean value.

For the simulations, two FinFET structures—the conventional PTM model and an underlapped FinFET—were also employed. We also investigate the effects of temperature on noise margins and static power for FinFET-based SRAM cells in this paper. FinFET has enhanced a number of performance measures, including efficiency, power, and space. FinFET has also been chosen as the favored transistor as it is unaffected by SCEs. Several FinFET-based SRAM cells, performance metrics, and cross-technology comparisons were investigated in this work. Consequently, for the purpose of building SRAM, the three-dimensional (3D) gate design of the nanoscale transistor, FinFET, is described.

➢ KEYWORDS:–

CMOS (Complementary Metal-Oxide-Semiconductor) ,SRAM(Static Random Access Memory), Static Noise Margin, FinFET(fin- field-effect transistor), Short Channel Effect

➢ INTRODUCTION:-

The integration method known as VLSI (Very Large Scale Integration) has been used by the researchers for a long time. A single chip made up of millions of transistors is called an integrated circuit (IC). VLSI is the name of this process. Innovations in the realm of VLSI provide creative approaches that lessen design constraints and increase circuit speed. These days, electronics follow the trend of being smaller.

The delay in pushing heavy loads on the bitline and wordline is the main factor affecting the SRAM subsystem's performance. Because of the magnitude of the main factor causing the whole power consumption in SRAMs on chip is leakage current in microprocessors built at nanometer nodes. Large standby power is produced by the exponential growth of leakage current. Conventional six-transistor (6-T) SRAM cells have scaling issues because to increased transistor leakage and parameter fluctuation. Subthreshold device leakage and well isolation leakage are two of the factors contributing to the SRAM array parametric standby leakage and the tunneling current of gate-oxide. The leaking power consumption of future SRAMs is the main cause for worry.

Modern Smart Gadgets (SG) are all made to be small, light, and portable. These devices often contain circuits for memory and processing. These days, memory is becoming an increasingly important component of most designs. Read stability is a commonly used criterion to evaluate an SRAM cell's ability to resist flipping during read operation. The hold stability is verified by installing the. largest square into the Voltage Transfer Characteristic (VTC) of the cross-coupled inverters inside the SRAM cell when the word line of the cell is switched off. The read and hold stability of SRAM cells is crucial to the design of FinFET-based SRAM. Therefore, an accurate and efficient computation of the Fin-FET based SRAM cell stability is needed during the design phase to ensure optimal SRAM operation and a high cache system yield. The Static Noise Margin (SNM) is a commonly used metric. The key challenge in growing SRAM technology is to consistently maintain a sufficient Read Noise Margin (RNM).

➢ FinFET TECHNOLOGY:-

One of the most suitable FET kinds on the market right now is finFET technology [16]. This enables faster simulation and execution of transistor applications in the analog and digital domains. FinFET seems to be a better option for nano electronics applications in the future due to its tiny susceptibility, low power consumption, low production costs, and outstanding performance [17–18]. Bulk CMOS transistors can be swapped out for FinFETs [19]. This technology is a good fit for memory subsystem architecture because to its low leakage current or standby power [20].

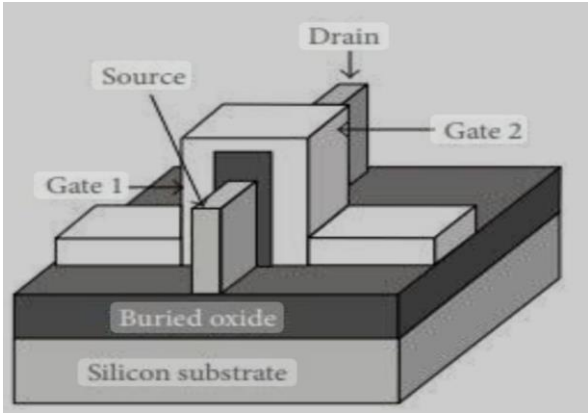

Fig 1: FinFET Structure

Fig. 1 mentions the diagrammatic depiction of FinFET. FinFET gets its name from the many perpendicular channels that resemble a fish's "Fin." It is constructed on a substrate and is also referred to as a multi-gate device (MGD). The gate is placed on one, two, three, or all four sides of the channel depending on whether a twin gate configuration is required.

On the silicon surface, the source or drain area takes the shape of a fin. A multi-gate transistor is another term for a FinFET. The following domains are covered by the FinFET model:- SiO2's gate-oxide region ; Region of heavily doped polysilicon ; Silicon fin with low doping ; The source-to-drain contact region is heavily doped.
There are two modes of operation for FinFET transistors: tied-gate (TG) and independent-gate (IG).

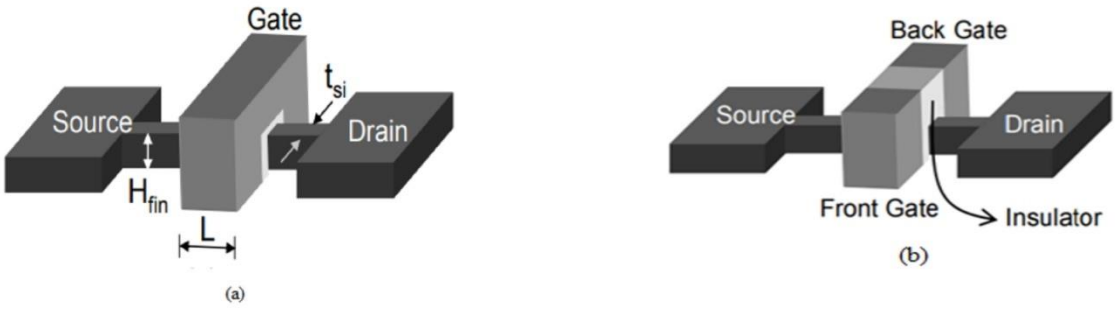

Fig 2 (a) TG FinFET 3D View & (b) IG FinFET 3D View

The FinFET TG and IG mode is shown in three dimensions in Fig. 2. In TG-mode, there is just one control signal (CS) that connects to the front and rear gates (FBGs). The TG FinFET design is simpler because of the shorter FBG. The TG-mode's increased gate-to-channel coupling allows it to avoid the SCEs. By binding with the N-type BGs to ground and integrating the P-type parallel FinFET, the IG-FinFET achieves similar increasing and falling delays.

The two FBGs are linked to separate control signals in the IG-mode. FinFET devices provide faster switching speeds and a higher current density than CMOS technology. Additionally, by lowering the off-state leakage, the SCEs are controlled. FinFET architectures provide a multitude of design options. It can function in several modes, such as hybrid, low power, TG, and IG. Among the advantages of FinFETs are the following: - inability to identify channel doping ; superior matching and exceptional SCE control ; Density scaling beyond planar devices (less than 20 nm); Smaller and more efficient in producing current ; Enhanced Profit and Minimal Cost

➢ SRAM Memory:-

Static RAM is a type of RAM that stores data in a fixed format until it is powered on. At Fairchild Semiconductor, Robert Norman invented semiconductor bipolar SRAM in 1963. In 1964, John Schmidt invented the metal-oxide-semiconductor SRAM (MOS-SRAM) at Fairchild Semiconductor. It was a 64-bit MOS p-channel SRAM.SRAM has been the main engine powering every new CMOS-based technology production processes since the development of CMOS in 1959.

Utilizing a transistor gate and tunnel diode latch, IBM engineers Eugene Schlig and Arnold Farber created a hard-wired memory cell in 1964. They replaced the latch with two transistors and two resistors to create what is now referred to as the Farber-Schlig cell. That year, they submitted an invention disclosure, but it was first denied.[5][6] In 1965, Benjamin Agusta and his colleagues at IBM created a 16-bit silicon memory chip with 80 transistors, 64 resistors, and 4 diodes, based on the Farber-Schlig cell.

The Intel 3101 was the company's first product, an SRAM memory chip meant to take the place of bulky magnetic-core memory modules. Its 64-bit capacity (although in early versions, only 63 bits could be used owing to a glitch) was based on bipolar junction transistors. It was designed using rubylith.

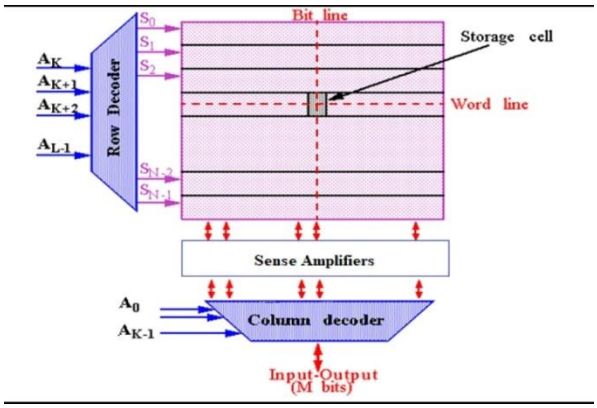

Fig 3 Architecture of SRAM Memory

A single row contains many words that are selected simultaneously. Address words are arranged in rows and columns, separated by addresses. To perform read or write operations, only one row of memory is enabled by the row address, while the column address selects one row from the given row. The storage cell, often referred to as the bit-cell or 1-bit memory cell, has two basic operating modes and two cross-coupled inverters in its latch circuit. The data in the storage cell can be represented using the logic "1" or "0". SRAM cells can operate in three different states. An SRAM memory cell normally consists of two access transistors and two simple cross-coupled inverters connected back to back [23].

When a word line (WL) is engaged for read or write operations, access transistors connecting it to complementary bit line (BL) columns are turned on. Many advantages of this circuit

architecture include medium power consumption, low leakage current, very low static power dissipation (SPD), and quicker data access.

➢ SRAM Cell Performance Metrics Using FinFET Technology:-

A: Read Noise Margin (RNM)

RNM is frequently used to gauge how resistant an SRAM cell is to flipping during read operations .For FinFET-based read stability (high RNM), Pull-down FinFETs , or SRAM cells, are usually more robust than access FinFETs. The pull-down transistor, or n FinFET, may be enlarged to enhance the read margin, although doing so comes with an area cost.

Alternatively , the gate length of the access FinFET reducing the write margin and lengthening the "WL" latency. To prevent inadvertently writing a 1 into the cell when attempting to read a stored "0," which might cause a read upset, the Fin-FET device must be carefully sized. The Cell Ratio (CR) 5 (W1/L1) / (W5/L5) is as shown in figure 4.

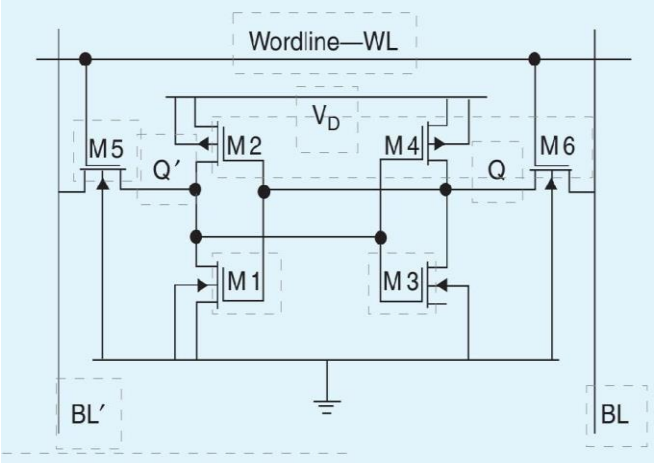

Figure 4 : 6T SRAM cell

Less cell ratios result in a greater voltage drop across the pull-down FinFET, which in turn requires a lower noise voltage at the "0" node to trip the cell. In the event of a read operation, the conducting access FinFET is positioned parallel to the pull-up PMOS, which reduces the static transfer characteristic's gain and increases the cell's resistance to noise.

B: Static Noise Margin (SNM)

Static Noise Margin (SNM), which measures the cell's resistance to flipping during a read operation, is a key indicator of stability .The biggest square within is used to compute SNM. The FinFET-based SRAM cross-coupled inverter characteristic (BL = BL', and WL=VD= VD) observed under read conditions. The commonly used metric to assess the stability of SRAM bit cells is the Static Noise Margin.

A high Vth indicates a low drive current in these devices, which makes write operations more challenging and raises the SNM. Just one Using high Vth devices at the expense of performance is one way to create a low power cell with good stability. In the access and pull-down n FinFETs, it is observed that the SNM is the least susceptible to the fluctuations and the most sensitive to threshold voltage variations with in the p FinFET pull-up device. Since the impact of Lg variation on Vth is negligible for FinFETs , its influence on the SNM is also negligible.

C: Write Noise Margin (WNM)

The greatest bit line (BL) voltage that may change the state of a FinFET-based SRAM cell while maintaining a high bit line bar (BL') voltage is known as the Write Noise Margin (WNM). More WNM indicates more stability. The node storing "1" can discharge more quickly by using a stronger access FinFET and a weaker pull up (p FinFET), which facilitates

A speedier version of "0" The highest BL' voltage that can reverse the cell state while maintaining BL at a high level is the write margin. Hence, at the expense of cell area and cell read margin, the write margin increases with a strong access and a weak pull up FinFET.

D: Power and Delay

The FinFET SRAM cell's power dissipation evaluates the cell's suitability for use in portable devices. The minimal access overhead of the FinFET-based SRAM is its primary benefit time and power loss as a result of the FinFET device's leakage current and low SCEs. A high driving current shortens the access time but increases the SRAM cell's power dissipation. The propagation latency in SRAM is influenced by wire delays and column height. Therefore, segmentation is used to lessen the hold-up.

A device's power-delay-product is constant , therefore raising one causes the other to decrease and vice versa. The FinFET technology in the SRAM cell can be upgraded to reduce latency at the expense of a little bit more power dissipation. However, leakage currents must be kept to a minimum in order to limit power dissipation, which calls for a longer channel or a higher transistor. Cutoff voltages. Higher latency is the outcome of longer channel lengths, and these two performance metrics are trade-offs.

E : Power Delay Product (Pdp):-

The transient analysis performance of SRAM cells is used to calculate PDP. It is a measurement of a circuit's energy usage. PDP is defined as the product of average power and gate delay. Additionally, PDP gives the processor that runs at a lower frequency preference. PDP for read and write operations should be reduced in an efficient SRAM cell. The extent of by optimizing the transistor size, the transistor is configured to achieve minimal power consumption while minimizing delay, all without increasing power consumption.

➢ Design of FinFET - Based SRAM Cell : -

The 6T (6Transistor) SRAM is composed of dual access FinFET transistors and two cross-coupled (2-CC) inverters [26]. The 2-CC inverters consist of four transistors: XM3, XM4, XM5, and XM6. Every bit in SRAM is kept in these four FinFET transistors. The two access FinFETs are (XM1, XM2), and the source terminals are linked to BL and BLB (BL Bar). The 6T SRAM cell is a widely used basic cell because of its smaller size. The dual access FinFETs are turned on when WL = 1 and the bit lines are connected to a latch that can perform a read or write operation. The access transistors go into the OFF state and BL, BLB are cut off from the latch at WL=0. Fig. 5 shows the schematic design of the FinFET-based SRAM 6T cell.

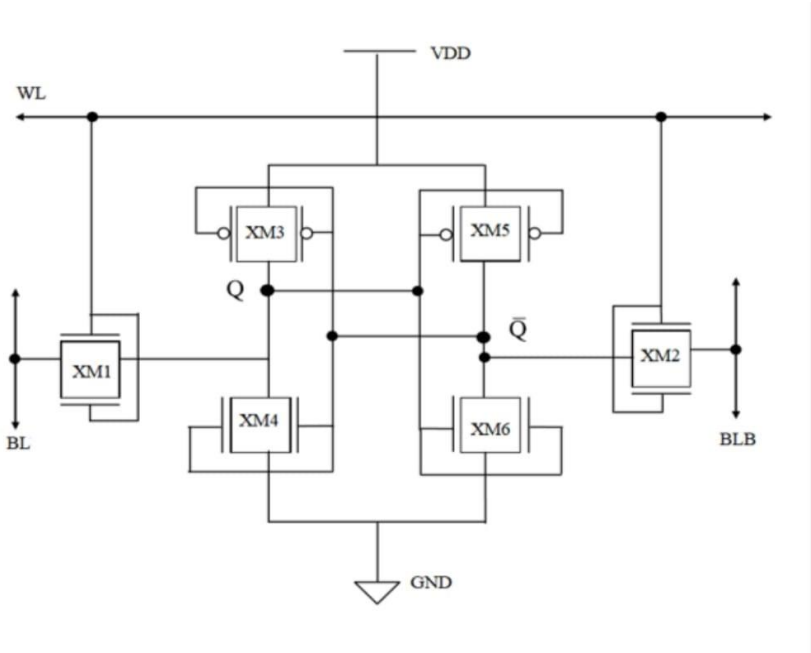

Fig 5 : FinFET 6-T SRAM Cell

The three fundamental operations are read, write, and hold [27–28]. In hold mode, WL is glued to the ground (GND). Consequently, the transistors XM5 and XM6, which switch off, divide the bit lines from the latching circuit.

The remaining transistors (XM1, XM2, XM3, and XM4) form a latch structure that holds stored data until it is separated from the thin lines. When in read mode, pre-charge the bit lines to VDD. Furthermore, link WL with VDD. This activates the XM5 and XM6 transistors. XM1 and XM4 are in the OFF state, whilst XM3 and XM2 are in the ON state, if Q = 1 and = 0. Consequently, the voltage levels of BLB and BL discharge and remain at VDD.

Connecting WL to VDD activates the transistors XM5 and XM6 while the write mode is active. After then, the node's voltage level starts to rise to the point where Q is high enough to turn on the transistors XM4 and XM2, at which time Q decreases.

➢ Design Problems with SRAM Cells Based on MOSFETs :-

To control Short Channel Effects (SCE) in MOSFET devices scaling into the sub-50 nm actual currents of subsurface leakage, strong super-halo implantation and heavy channel doping are required. In the on state, a strong transverse electric field exacerbates sub-threshold swing and increases parasitic junction capacitance; extensive doping lowers mobility due to impurity dispersion.

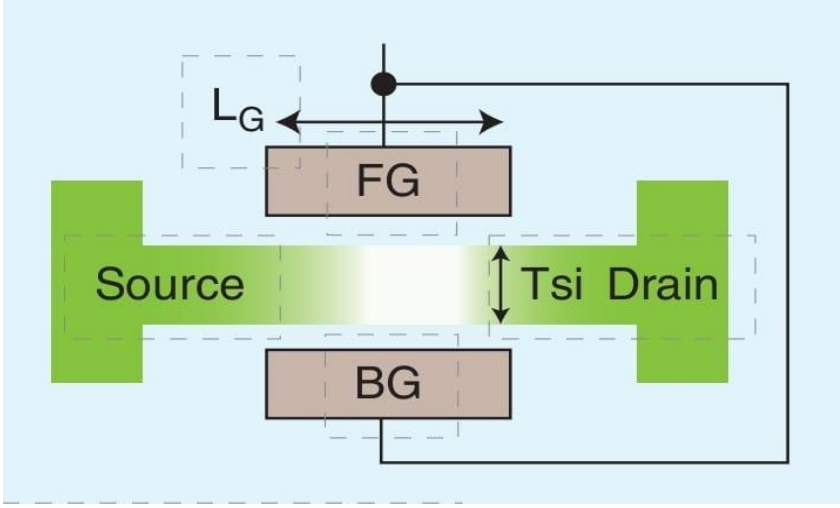

Fig 6: Double Gate FinFET

As a result, for a given off-state leakage current specification, the on-state drive current degrades. Band-to-band tunneling raises the off-state leakage current between the drain and the body. Threshold voltage (Vth) variability.Random dopant oscillations provide an additional cause for concern for nanoscale bulk MOSFETs.

As variations increase, it becomes more difficult to achieve near-minimum SRAM cell stability for large arrays in embedded low-power devices. On the other hand, when transistor size increases, density—the main driver of scaling in the first place—is compromised. Access time is impacted by wire delays and column height. Segmentation is often used to speed up arrays.

The overhead area of sense amplifiers greatly rises when bit-line height is progressively lowered. In a bulk MOSFET-based SRAM array, an exponential increase in leakage current generates large standby power. Furthermore, mismatches in the power of different SRAM cell components result from variances in processes.

Such a mismatch might result in parametric failures, which would lower the yield of the design. Building robust and low-power SRAMs is one of the main problems in nanoscale technology because of the large leakage current and increased parametric variation.

Because of increased short channel effect (SCE), scaling single gate bulk CMOS devices beyond sub-50nm node is becoming increasingly challenging. Ultrathin body double-gate MOSFET (DGFET) devices are advantageous for sub-50nm technologies due to their superior scalability, greater on-current, and increased resilience to SCE compared to single gate devices. Furthermore, the low junction capacitance of the DGFET significantly reduces the circuit delay. Furthermore, DGFET devices have a mild doping on their bodies, and the metal gate work function is mostly utilized to control the 1 Vth 2 threshold voltage. Random dopant fluctuation (RDF) causes the minimally doped body to remove changes in Vth.

➢ FinFET Device with Underlapped:-

The FinFET device is modeled in our study using the Predictive Technolog Model (PTM) as a self-aligned Double Gate (DG) MOSFET, minus the fin extension areas. This model is enough for comprehending the features of the FinFET device and appreciating its advantages. Figure 7 depicts a typical underlapped FinFET device topology.

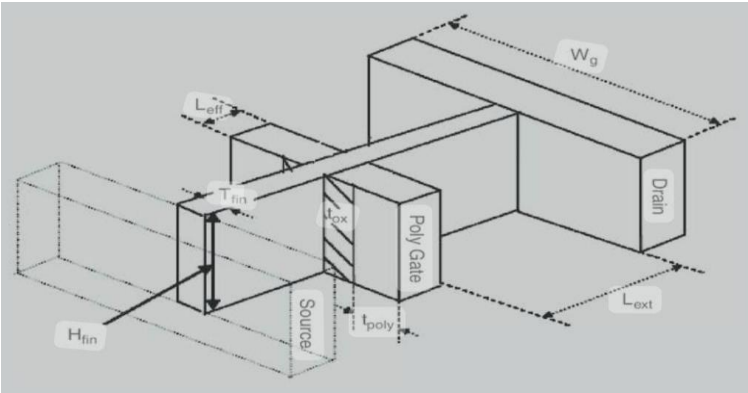

Fig 7: Underlapped FinFET Device

Nevertheless, the fabrication of abrupt junctions and thin fins is hindered by technological limitations [33]. Consequently, FinFET requires a modification to the double gate structure seen in the PTM model [23] in order to accommodate the fin extension areas that arise from technical constraints.

The physical separation of the gate and drain area, which keeps the gate from straggling the drain, results in reduced Gate Induced Drain Lowering (GIDL) in the underlapped FinFET structure with fin extension regions. The channel of a Fin-FET device is essentially undoped (completely depletion), as was previously described, to prevent Vth fluctuation and mobility

deterioration as a result of doping changes. If left undoped, the FinFET's extension regions provide a high resistance to the drain current, which significantly limits the use of the device in low-power applications utilizing low voltage sources. This is anticipated to result in a significant degradation of the FinFET's current driving capacity.

Despite these factors, the FinFET decreases leakages more than the overlapping device (PTM) and operates in a direct process flow from the CMOS technology, making fabrication simple and low in overhead expenses. Additionally, the fin extension raises the voltage on the source side just outside the channel above ground. As a result, the drive current is further decreased and the gate's ability to flip the channel is effectively diminished:-

a.) Diverse Underlapped FinFET Parameters:

The following are the parameters shown in Figure 7: Leff: Length of Gate, Tfin: The fin layer's thickness, Hfin is the fin's height, and tpoly is the polysilicon layer's thickness. above the gate oxide tox: The oxide film's thickness, Length of the fin extension zone between the gate-drain or gate-source region is measured by Lext. Wg: The source/drain areas' width WS/D stands for source/drain contact region length.

b.) FinFET Process Variations Analyzed using Monte Carlo:

The observed random distribution of FinFET device characteristics can be attributed to changes in W/L in MOS transistors caused by the photolithographic process' low precision. The differences between W and L are not correlated because L is specified in the poly and source/drain diffusion processes, and W is calculated in the field oxide step.

The process parameters that can vary in FinFET-based SRAM are the threshold voltage (Vth), fin thickness (Tfin), and fin width (Wfin). These changes have an impact on latency, power usage, and noise margins. Memory architectures have 6s variations in mind [28]. We performed Monte Carlo simulations on HSPICE for 1000 sample values, assuming 3s equal to 10% of the mean value, to evaluate the effect of process parameters on FinFET SRAM.

c.) How Temperature Affects FinFET Performance:

Power dissipation has become a crucial bottleneck in the design of nanoelectronics due to increased packing density. An increase in local temperature may cause a circuit. The malfunction and may also affect dependability, power, and performance. A FinFET's drive current drops by around 4% and its interconnect (Elmore) latency rises by about 5% with every 108 C increase in temperature [16]. A CMOS chip's power density, or power dissipation per unit area, is expressed

as = CVD 2f, where C is the node capacitance per unit area; it is determined by the signal's average switching activity, where f is the clock frequency and VD is the supply voltage.

A temperature increase causes the leakage current to increase exponentially (a difference of 30 degree C will effect the leakage by 30%), which causes the power dissipation in a FinFET device to increase significantly. This in turn raises the temperature even more, and so on until thermal runaway happens. As a result, one of the most crucial performance metrics for upcoming VLSI circuit designs is temperature.

➢ Simulation Result & Discussion:-

A simulation of the various SRAM technologies is given in this section.Propagartion latency, power dissipation, and PDP are used to evaluate the performance of these SRAM technology. The 6T- SRAM cell simulation results are displayed in Figure 8.

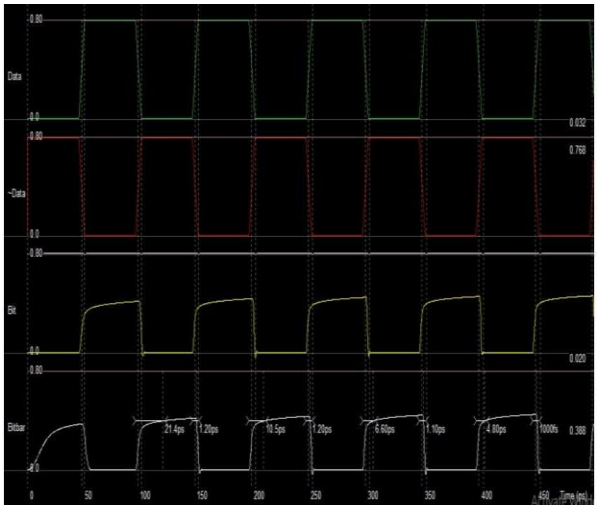

Fig 8: Simulation Result of 6T-SRAM Cell

Traditional CMOS-Based SRAMcell designs are compared with the performance of the 6T SRAM using FinFET. FinFET-based SRAM architectures are seen to offer reduced PDP, low power consumption, and minimal propagation latency. Additionally, the efficacy of the suggested design is evaluated against the conventional state of the art using a variety of stability metrics, including read, write, and noise margin.

➢ CONCLUSION & FUTURE WORK:-

In this study, we improved the performance resilience of the cell by examining the trade-offs associated with the design of SRAM based on FinFETs. Analysis has been done on the SNM, RNM, WNM, and static power fluctuation with driver, load, and width of access. Moreover, the

effect of process variation on the SRAM cell's performance was investigated using Monte Carlo simulation using HSPICE.

This survey looks at a number of SRAM designs that utilize FINFET technology. The study that is being offered shows why utilizing a FINTEP to construct SRAM is better than using a CMOS SRAM cell, since the former has shorter delay in both operations and higher static power dissipation. FinFETs are superior to bulk MOSFETs in a number of ways. While the manufacturing process for DGMOSFET is complex, the fabrication flow used to manufacture FinFET is similar to that of the conventional SOI CMOS approach.

Compared to earlier designs, the FinFET structure is a more densely packed DG MOSFET. To eliminate the SCEs, FinFET based SRAM models are provided. These models exhibit a discernible reduction in both power dissipation and leakage current when juxtaposed with conventional MOSFET-based SRAM cells.

Thus, this review contributes to our understanding of the behavior of FinFET-based SRAM in high-power, low-power situations. Fastness, low leakage, and outstanding performance are crucial. Additionally, a variety of contemporary electronics applications, such as SD-RAMs, CPUs, and mobile technologies, are ideally suited for this FinFET-SRAM design. In several low power CMOS circuit applications, they are also utilized. A Multi-Fin FinFET device might be used in the future to enhance the device's driving capabilities.

Future research in nanoscale technology for finfet-based SRAM cells may focus on pushing the boundaries of downsizing and scalability by investigating novel materials or architectures, enhancing stability against process fluctuations, and refining the design for improved performance. The development of novel methods for large-scale system integration, testing, and manufacture may also be the subject of research. Furthermore, it may be fascinating to look into how cutting-edge technologies like neuromorphic or quantum computing affect SRAM architecture.

➢ Acknowledgement:-

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