DESIGN A 3D NANOWIRE FET WITH CORNER SPACER APPLICATION

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Abstract

The primary cause of the total device capacitance in nanoscale FETs is progressively turning out to be the parasitic capacitance, which lowers the performance of the device and circuit. The use of multi-gate FETs, including FinFET and gate-all-around FETs, exacerbates this problem. Corner spacers are a concept for gate-all- around nanowire field-effect transistors that minimize ON-current degradation while significantly reducing parasitic capacitance. We show that, compared to the device equipped with full nitride spacers, the parasitic capacitance of a precisely designed corner spacer in a nanowire FET may be reduced by more than 80%. When compared to the full spacer, the corner spacer design in the circular oscillator stage has a delay and energy usage that are less than 40% of the latter.-5.This work shows how manufactured spacers can be used to improve performance and allow for additional scaling.

Index Terms— Corner spacer, nanowire FET, parasitic capacitance.

Introduction

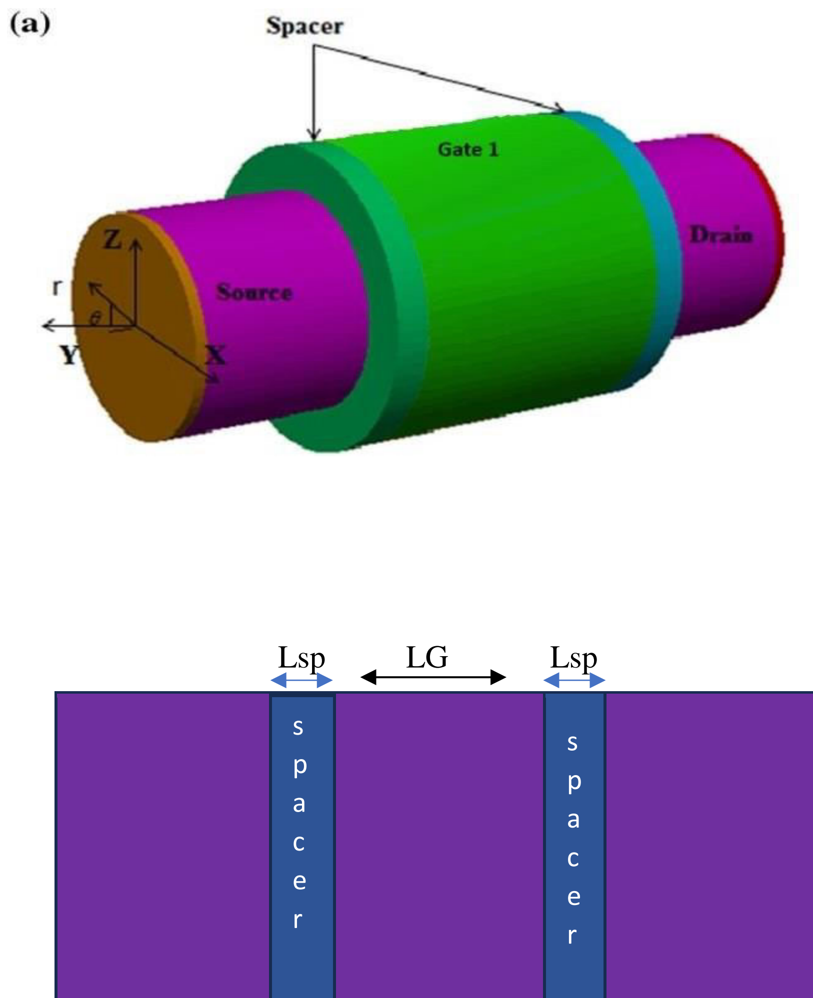
FINFET is the technology currently used in the industry for very-large-scale integrated circuits with a node size below 28nm [1]–[4]. FINFET technology is currently used in the industry for very-large-scale integrated circuits with a node size below 22 nm. [5] By adopting the quasi-planar design of FinFET, it is possible to improve the ON-current per device size.The fins are increased in height, hence lowering the total length of the tool. The fin height was raised from 26nm at the 12-nm node to 32 nm at the 16-nm node [2], [3]. The short-channel [7]. Because the FinFET has several gates that balance the thin, completely depleted channel, it performs better in short channels than the single-gate planar MOSFET. To provide satisfactory performance FinFET technology involves the measurement of the channel's thickness Results in a reduction in the turn – on voltage. while maintaining the same OFF-current, resulting in a larger gate overdrive voltage and thus, a greater ON- current.

3-device's performance by increasing the effective gate length through the use of a systematic source-drain underlap doping design. However, the ability to scale the beam of the fin may be limited to 6 nm due to difficulties encountered during the manufacturing process. To improve short-channel capability, a systematic sou3-device's performance by increasing the effective gate length through the use of a systematic source-drain underlap doping design.-[7]-drain underlap doping design can be implemented, which results in a longer effective gate length. Researchers have also investigated different spacer plan, typically with a larger dielectric constant (κ), to reduce the resistance caused by underlap.[10]-[11] In nanoscale FinFETs, A significant proportion of the total capacitance is expected to be made up of parasitic capacitance. The parasitic capacitance should decrease as a result of scaling between the gate edge and the contact cable.

DEVICE STRUCTURE AND SIMULATION SETUP

Displays a three-dimensional diagram of a nanowire field-effect transistor (FET) featuring a corner spacer, along with the matching conic-sectional perspective. The gate ratio of the tool is four times the specified gate length. The term "technology computer-aided design (TCAD)" describes the application .The simulation setup was adjusted to match the experimental data, which included gate lengths ranging from 15 to 35 nm. To capture the physical processes occurring in the device, the modified local-density method quantum correction, band-to-band tunneling, contact resistance, low field and doping-dependent mobility drop carrier creation and recombination, and velocity saturation and overshoot were employed.

carefully designed to match thebehavior of drain-induced barrier lowering (DIBL) as the gate length scaled. LG = 15 nm, fin pitch PF = 62 nm, fin height HF = 45 nm, fin width WF = 24 nm, and contact pitch = 100 nm are the dimensions of the device. A 10-nm gate length nanowire FET device is used in this work.



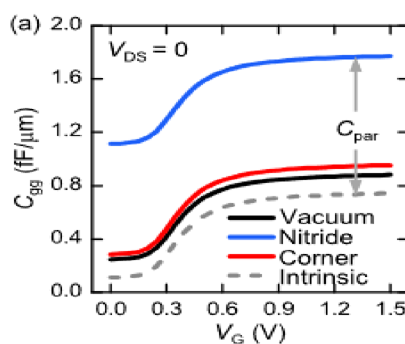
An advanced technology that uses the special qualities of nanowire to improve electrical performance is a 3D Nanowire Field-Effect Transistor (FET). A semiconducting nanowire channel (made of materials like silicon) with lengths and widths ranging from a few of nanometers is usually a part of its structure. To enable current flow, source and drain electrodes composed of metals like gold or platinum are positioned at the ends of the nanowire. The gate electrode is often composed of metals or highly doped polysilicon. It can be arranged in a gate-all-around, top-gate, or bottom-gate arrangement. To ensure efficient gate control, a gate dielectric material made of high-k materials like hafnium dioxide this gate from the nanowire.

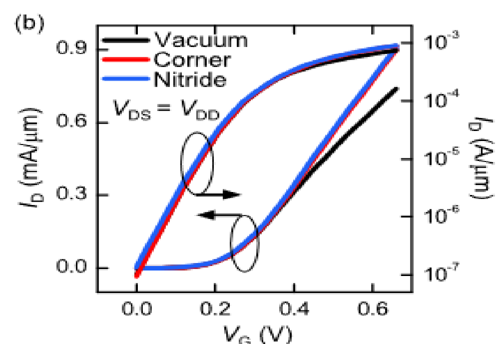
CATEGORICAL DATA PARAMETERS

Symbol	Value	Quantity
Lg	15nm	Gate length
EOT	0.8nm	Effective oxide thickness
T_{ox}	3.52nm	Physical thickness of oxide
E_{Hk}	26nm	Dielectric constant of high-k oxide
E_{COR}	9.45nm	Dielectric constant of corner spacer
E_{SP}	1nm	Dielectric constant of outer spacer
d_{NH}	15nm	Diameter of nanowire
L_{SP}	8nm	Length of spacer
T_{SP}	15nm	Thickness of outer spacer
L_{COR}	2.5nm	Length of corner spacer
T_{COR}	9.5nm	Thickness of corner spacer
T_G	11.68nm	Thickness of gate
T_{EPI}	12nm	Thickness of S/D epi
N_{SD}	$3x10^{20}$nm	Doping in S/D region
N_{CH}	10^{36}nm	Channel doping
V_{DD}	0.82	Supply Voltage

UNDERLAP DESIGN

To maximize the ON-current (ION) at IOFF = 50 nA/µm, we optimize the nanowire's source/drain doping. The device's short-channel performance is improved and the OFF-current is decreased The effective gate length increases when the underlap length is increased.(Leff = L G + 2LUN) [8]. The parameters of I D-VG at IOFF = 50 nA/µm.The criterion of iso-IOFF is met. by changing the gate metal's work function. When ions are present in underlap devices, a balance must be made between the boost in resistance in the underlap regions and the decrease in threshold voltage (VT), which results in a higher gate overflow voltage (VG – VT). The increased sub-threshold swing caused by a longer underlap region at iso-IOFF causes the threshold voltage to drop, raising the gate overdrive voltage. With an increase in underlap length comes an increase in underlap resistance. The performance metrics of short-channel devices, such as drain current (ION), subthreshold swing (S), and drain-induced barrier reduction (DIBL),for different underlap lengths. Raising the LUN causes S and DIBL to decrease, which is related to the rise in Leff. S and DIBL values first decrease quickly before reaching a saturation point. The equivalent S values at LUN values of 0, 1.5,2.5, 5, and 4.5nm are, respectively, 104, 75, 70, and 66 mV/decade. S and VT decrease to create the first rise in ION, but when LUN increases, underlap resistance increases to cause a decrease in ION. The underlap length of approximately 3.0 nm is when the greatest value of ION at IOFF = 101 nA/µm occurs. This is true for all designs of spacers. We use a 1.5 nanometer-sized LUN for the remaining section of the same page.

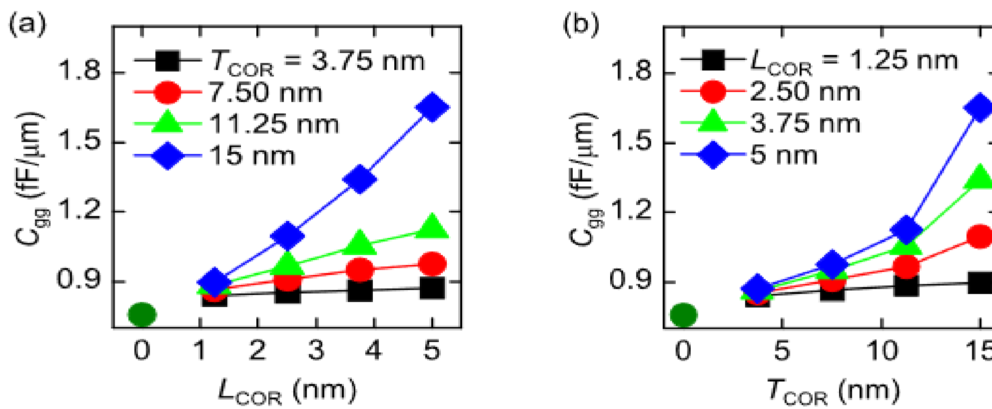




CORNER SPACER DESIGN

The use of various spacers in nanowire FETs has a significant impact on their efficiency considering the nanowire FET's parasitic capacitance varies greatly depending on the spacer design, with complete nitride spacers having a Cpar of around 80%, nitride corner spacers having a Cpar of around 18%, and vacuum spacers having a Cpar of around 21% relative to the intrinsic capacitance. The use of nitride corner spacers results in an approximately 60% reduction in Cpar compared to complete nitride spacers.

The device's subthreshold properties are not significantly impacted by the spacer design, but the ION (current flow) is. Comparing the vacuum spacer nanowire FET to the whole nitride and nitride corner spacer nanowire FET, the ION of the former is around 12% lower. When nitride corner spacers are used instead of full nitride spacers, the gate-to-gate capacitance (Cgg) of the nanowire FET significantly decreased, but the ON current (ION) is not decreased. The drop in both the gate-to-epi capacitance (Cepi) and the outer fringe capacitance (Cof) causes the nitride corner spacer nanowire FET's parasitic capacitance to decrease.



SCALING

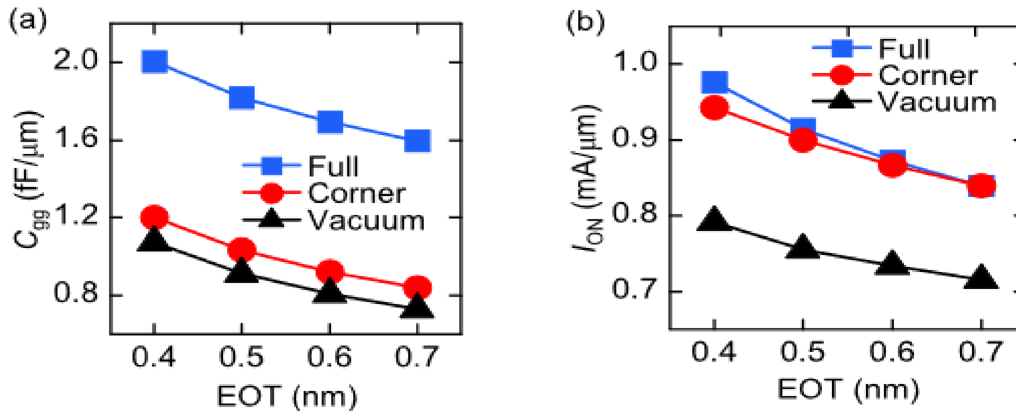
shows that while the parasitic capacitance components (Cof and Cepi) stay constant, the intrinsic capacitance (Cox L G) diminishes, causing the parameter Cgg to fall linearly with decreasing gate length. The total nitride, nitride corner, and vacuum spacers have parasitic capacitances of 959, 148, and 77 attofarads (aF), respectively. When LG (gate length) is 60 nm, The nitride corner spacer's Cgg (gate capacitance) is around 25% smaller than the complete nitride spacer's, and it is about 45% smaller when L G is 20 -3D MOSFETs with a total capacitance of nm include FinFET and gate-all-around nanowire FET.

consists of certain components that are width-independent and others that scale with the device's will. Figure (a) shows a favorable relationship between ION and reductions in LG.The nitride spacer nanowire FET's total ion current is similar to that of the nitride corner spacer. On theother hand, the vacuum spacer's ion current is much lower—roughly 17% Lowering (Effective Oxide Thickness).At LG = 45 nm and often around 14% lower at LG = 20 nm.As the effective oxide thickness (EOT) drops, the value of Cgg rises, as seen in Figure 8(a). Because of the greater contribution of parasitic capacitance from CoF and Cepi, the capacitance of the entire nitride spacer is bigger than that of the nitride corner and vacuum spacer devices. As seen in Figure (b), there is an inverse relationship between the rise in ION and the drop in EOT. While ION is significantly lower in vacuum spacer devices than it is in full nitride and nitride corner spacer devices.

$$EOT = \left(\frac{3.9}{K_{high-k}}\right)t_{high-k}$$

The channel resistance falls in parallel with a drop in the Effective Oxide Thickness (EOT). When the effective oxide thickness, or EOT, decreases, underlap resistance makes an important difference to the overall resistance. Due to the increased underlap resistance, the Ion with EOT (Ion/EOT) rise for vacuum spacer devices is smaller than that of full nitride and nitride corner spacer devices. Both the nitride corner spacer and the vacuum spacer device's gate-to-gate capacitance (Cgg) show parallelism; however, the nitride corner spacer's Cgg rises at a higher rate (EOT) than the vacuum spacer device's.

$$EOT_{total} = (\frac{3.9}{K_{high-k}})t_{high-k} + t_{ox}$$



Nanowire Diameter Scaling

3-D MOSFETs, like FinFET and gate-all-around nanowire FET, have a total capacitance made up of certain parts that scale with the width of the device and some parts that are width-independent. More precisely, the oxide capacitance (Cox) in a FinFET, and gate-to-epi capacitance (Cepi).and outer fringe capacitance (Cof) all rise in direct proportion to the fin's thickness and height. The corner capacitance (Ccorner), however, doesn't change . The number of fins on a crab rises in direct proportion to its growth.

$$\frac{1}{C_{eq}} = \frac{1}{C_{high-k}} + \frac{1}{C_{ox}}$$

Epi Thickness Scaling

As the depth of the axial layer (TEPI) grows, the capacitance of the axial layer (Cepi) and, consequently, the gate-to-ground capacitance (Cgg) also increase, as illustrated in Figure 10(a). The cepi is composed entirely of nitride material.

Spacer Length Scaling

As the spacer's length (LSP) increases, the value of Cgg decreases. The properties of full nitride spacer and nitride corner spacer nanowire FETs are similar when the capacitance between the source-drain exponential regions and the gate edge increases.

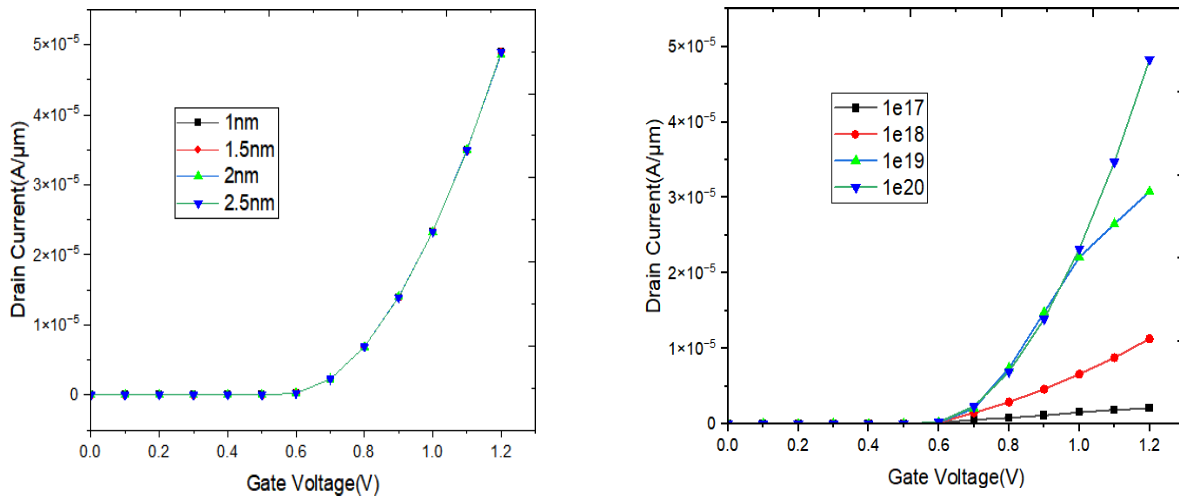
Gate Thickness Scaling

Shows that when the gate terminal thickness increases, so does the gate electrode's capacitance (Cgg).As the temperature variance (TV) grows, the coefficient of friction (Cof) and the coefficient of thermal expansion (Cepi) also increase, resulting in an increase in the thermal conductance (Cgg). Compared to the whole nitride spacer, the conductivity of the nitride corner spacer is significantly lower. There are parallels between the ion of nanowire FETs with full nitride spacer and nitride corner spacer.

AUTONOMOUS PERFORMANCES

It shows that the time delay of each stage in the ring oscillator of the complete spacer nanowire FET lengthens with a rise in the spacer material's dielectric constant. The capacitance of the entire spacer device is directly correlated with the spacer's dielectric constant. In the end, this raises the stage delay of the ring oscillator.The increase in ION is more significant than the increase in Cgg in the corner spacer nanowire FET. The stage delay decreases as the dielectric constant of the corner spacer increases. The oxide and nitride corner spacer has a delay in the ring oscillator stage that is approximately 12% less than that of the vacuum spacer device. The dielectric constant of the corner spacer has a linear effect on the growth of Cgg, but it has very little effect on the ION.

RESULTS & DISCUSSION



A major development in the field of high-performance and energy-efficient applications is the nanowire FET with corner spacer. There have been a number of important enhancements made to the design by adding corner spacers, which call for careful consideration and research. First of all, because of their high surface-to-volume ratio and superior gate control, nanowires provide additional advantages like improved electrostatic control and decreased leakage current when used as the transistor channel. This fundamental element lays the groundwork for improved transistor performance. The use of corner spacers accomplishes several important goals. By efficiently adjusting the size and form of the gate structure, these spacers improve gate control and lessen the effects of short channels. Furthermore, the proposed design's scalability and manufacturability has to be taken into account. The integration of corner spacers into nanowire FETs is a possible path for enhancing the state-of-the-art in semiconductor technology, provided that corner spacer integration is suitable with current semiconductor production procedures.

CONCLUSION

Our results indicate that in order to lower Therefore, a corner spacer design is required to reduce the parasitic capacitance without affecting the ON-current. This design uses a lower κ dielectric material to encircle the lower half of the gate sidewall and a higher κ dielectric material to be placed there. We observe that the addition of a corner spacer design reduces the parasitic capacitance by 45% in a nanowire FET with a gate length of 15 nm without causing an apparent decrease in the ON-current. Additionally, the ring oscillator stage's delay and energy consumption per cycle are decreased by more than 50% when compared to the use of a complete nitride spacer. Corner spacer design is able to reduce energy consumption and maximize efficiency for sub-20nm multi-gate FET circuits and devices. The trends presented in this paper can also be applied to stacked nanowire FETs. We anticipate that the design will improve the high frequency performance of multigate FETs, which are adversely affected by excess parasitic capacitance, by lowering unwanted capacitance in corner spacers.

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