RES MILITARIS Social Science Journal

VLSI IMPLEMENTATION OF A BARREL SHIFTER

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ABSTRACT:

A Barrel Shifter is a multiplexer based digital circuit. Several microprocessors incorporate it as a part of their ALU to provide fast shift operations. This paper deals with the design of Barrel Shifter using VLSI Technology. Four modules have been designed which consist of an inverter which forms an integral part of 2:1 Multiplexer and 4:1 Multiplexer and also used as control inputs, an AND gate used for arithmetic shifting, a 2:1 MUX used for collecting the falling bits and a 4:1 MUX needed to shift the data words left or right. There are three stages of 4:1 MUX with smaller 2:1 MUX preceding it in every stage. The modules have been designed in Schematic-edit and they have been simulated in Waveform-edit.

I. INTRODUCTION

A Barrel Shifter is a digital circuit that can shift a data word by a specified number of bits. It can perform shifting of N-bit data in a single cycle. A N-bit Barrel Shifter can shift data left or right by N-1 bits. In general, a Barrel Shifter can implement arithmetic shifting, logical shifting and rotation functions [10]. The signals for the input/output, and shift functions for a N-bit barrel shifter are given as follows:

Data In = (2x(N-1)) Bit
Shift Amount = ($\log_2 N$) Bit
Data Out = (N) Bit

The principal distinction between a barrel shifter and an ordinary shifter is the amount of bits being shifted at one time. A common shifter will usually shift only one bit per cycle whereas a barrel shifter can shift many bits per cycle. It can be implemented as a sequence of multiplexers. The number of multiplexers required is [nlog2(n)] , for a n bit word. Four common word size and the number of multiplexers needed are listed below:

16-bit — 16log 2 (16) = 16 x 4 = 64

8-bit — 8log 2 (8) = 8 x 3 = 24

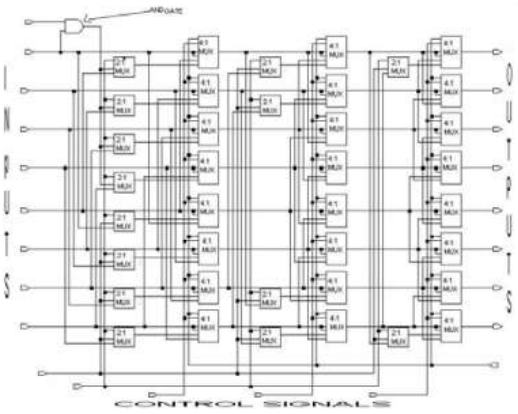

Fig: Block Diagram of 8 Bit Barrel Shifter

Consider a four-bit barrel shifter, with inputs A, B, C & D. The shifter can cycle through the order of the bits ABCD i.e. it can 'shift' all of the outputs up to three positions to the right and thus make any cyclic combination of A, B, C and D. This makes a barrel shifter a vital component in microprocessor (along with the ALU) [11].

II. METHODOLOGY

The design and simulation of the layout for N-bit Barrel Shifter is carried out by using VLSI technology . The functionality of the shifter includes arithmetic shifting, logical shifting, and rotation. The design is divided into smaller sections so that it becomes easy to build and test each function of the circuit separately for each section.

The first stage shifts the word bit by 4 bits, the second by 2 bits and the third by 1 bit shifting a total of 7 bits. A total of twenty four 4:1 multiplexers (8 for each stage) are used for designing purpose [09].

The Multiplexers at each stage would shift the bits according to the shift amount. Arithmetic shifting is needed and so AND gate is connected to the last four inputs in the first stage. The AND gate would copy the MSB (most significant bit) and shift it in according to the shift amount. For example if MSB is "one", it would be shifted in 4 times if the shift amount is 4 (only right shifting carries the MSB).

In Barrel Shifter, when shifting logically, the bits shifted "fall off" at the ends of the multiplexers. To rotate the bits, we need to "catch" these bits which are being lost. To do this, a 2- to-1 multiplexer is implemented in the circuit for every lost bit. Thus, the design requires twelve 2:1 multiplexers [10].

III. DESIGN APPROACH

1) CMOS Inverter

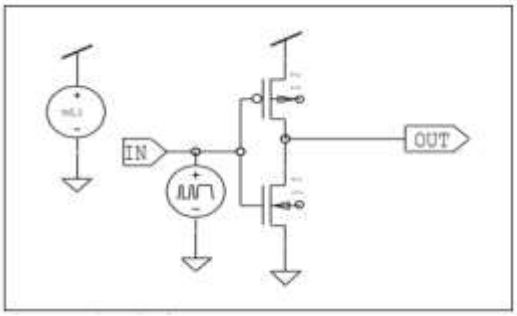

Fig III.1.a: Schematic of CMOS Inverter

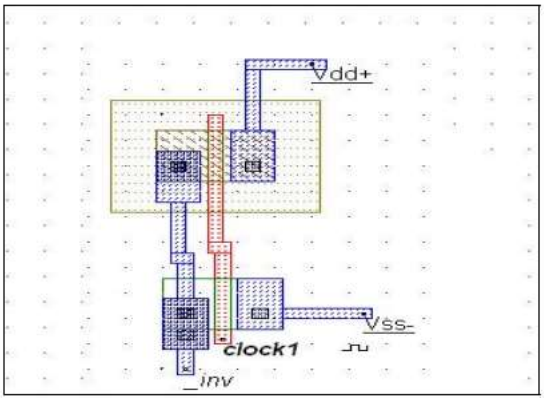

Fig III.1.b: Layout of CMOS Inverter

The inverter is implemented using P-MOS & N-MOS in series where IN corresponds to Input Bit and OUT corresponds to Output bit [1], [3].

2) CMOS AND Gate

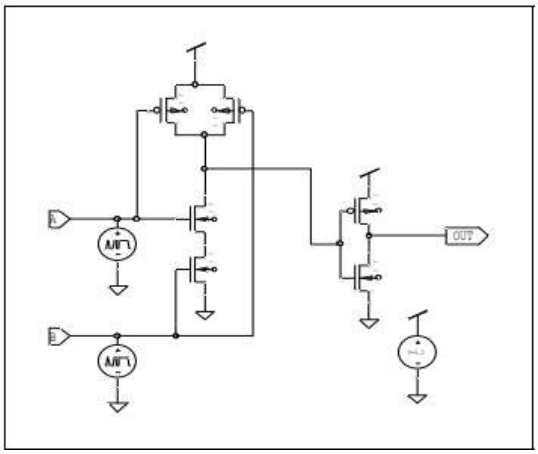

Fig III.2.a: Schematic of CMOS AND Gate

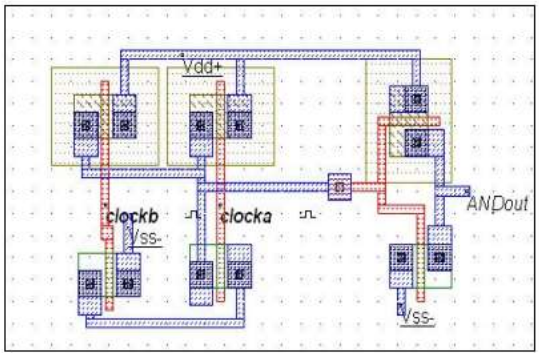

Fig III.2.b: Layout of CMOS AND Gate

The AND gate is implemented using two N-MOS structure in series, two P-MOS structure in parallel and one Inverter [1]. We have implemented AND gate by inverting the output of NAND gate. The Inputs are given to the gates of both N-MOS and P-MOS & output of NAND gate is fed as input to the inverter. VDD and Ground are connected to Source and Drain of MOS structures respectively [3].

3) CMOS 2:1 Multiplexer

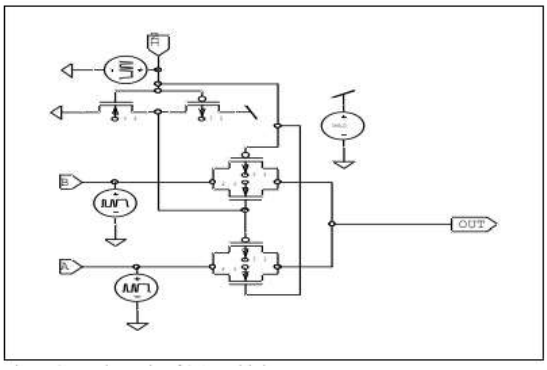

Fig III.3.a: Schematic of 2:1 Multiplexer

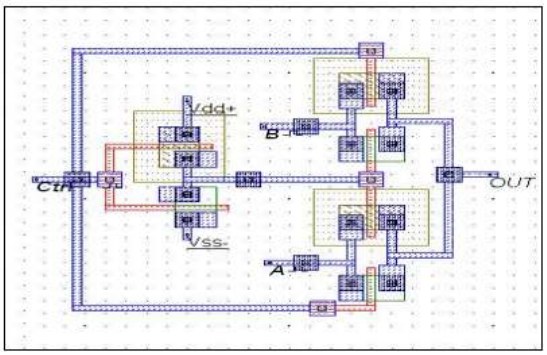

Fig III.3.b: Layout of 2:1 Multiplexer

In digital circuit design, the selector wires are of digital value. In the case of a 2:1 multiplexer, a logic value of 0 would connect B to the output while a logic value of 1 would connect A to the output. In larger multiplexers, the number of selector pins is equal to n where n is the number of inputs. A 2:1 multiplexer obeys the following a Boolean expression:

Z = (AS +BS')

Where A and B are the two inputs, S is the selector input, and Z is the output [13].

The implementation of 2:1 MUX uses 2 Transmission Gates. A & B are the input bits, IN corresponds to the control signal. The output is obtained depending upon the control signal.

4) CMOS 4:1 Multiplexer

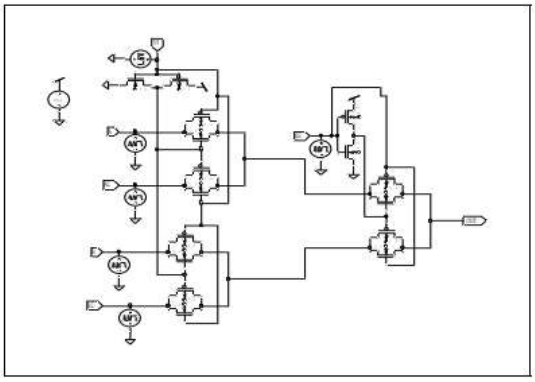

Fig III.4.a: Schematic of 4:1 Multiplexer

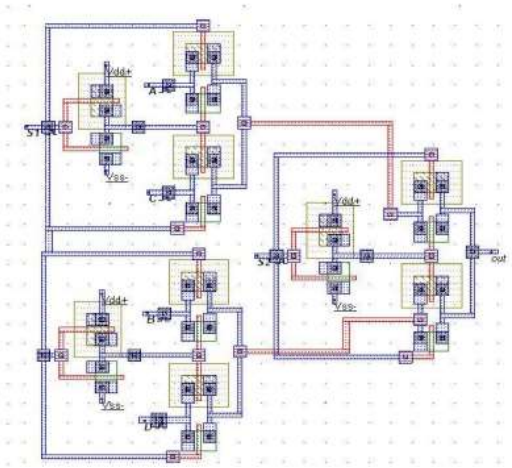

Fig III.4.b: Layout of 4:1 Multiplexer

4:1 MUX is implemented using three 2:1 MUX. A,B,C,andD are the input bits and S1 & S2 are the control signal. Now depending upon both of these the output is obtained [12]. The Boolean expression obeyed by the 4:1 Mux is as follows:

Z = AS1'S2' + BS1'S2 + CS1S2' + DS1S2

When S1 and S2 are both zero then input A will be selected. Similarly B will be selected when S1 is zero and S2 is one & so on.

IV. SIMULATION RESULT

1) CMOS Inverter

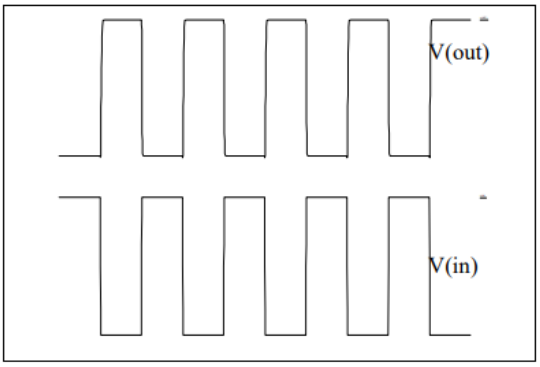

Fig IV.1.a: Schematic Result for CMOS Inverter

In the simulation we can see that when input is High output obtained is Low. Hence Output of Inverter is verified.

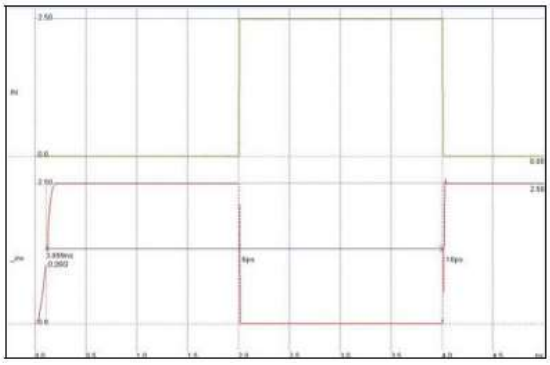

Fig IV.1.b: Layout Result for CMOS Inverter

2) CMOS AND Gate

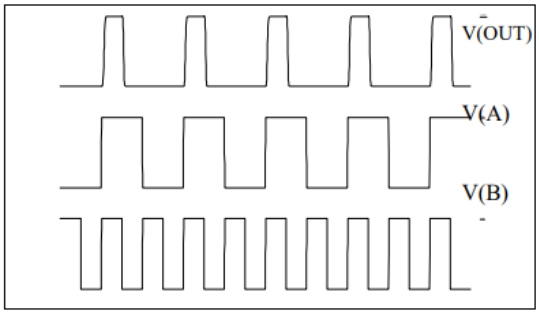

Fig IV.2.a: Schematic Result for CMOS AND Gate

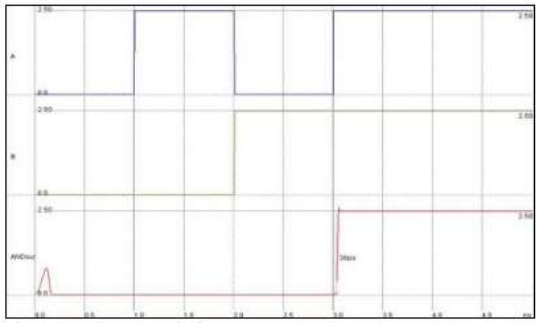

Fig IV.2.a: Layout Result for CMOS AND Gate

Here, we see that the output of the AND gate is High whenever the inputs A & B are High. The output is Low when either of the inputs is Low. Again the AND gate works as expected [8].

3) CMOS 2:1 Multiplexer

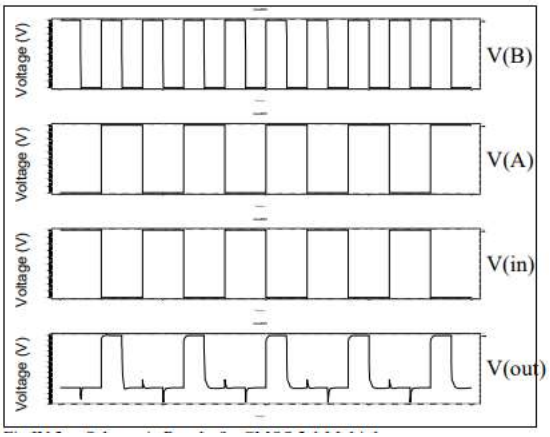

Fig IV.3.a: Schematic Result for CMOS 2:1 Multiplexer

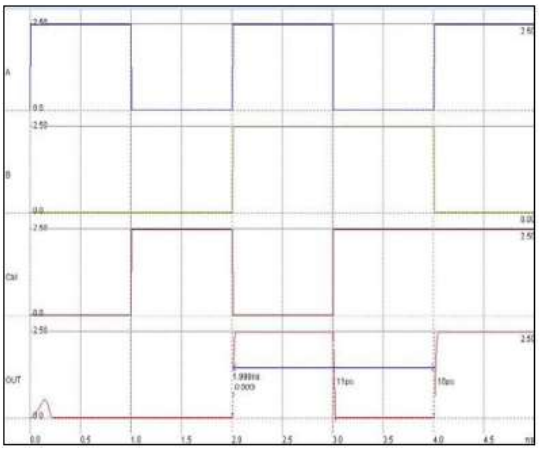

Fig IV.3.b: Layout Result for CMOS 2:1 Multiplexer

S	A	B	Out
1	1	X	A
1	0	X	A
0	X	1	B
0	X	0	B

Fig IV.3.c: Truth Table for CMOS 2:1 Multiplexer

In this simulation we see that with different control signal value [V(S)], we obtain different output. Explicitly, when V(S) = 1, V(A) is selected and when V(S) = 0, V(B) is selected [6].

4) CMOS 4:1 Multiplexer

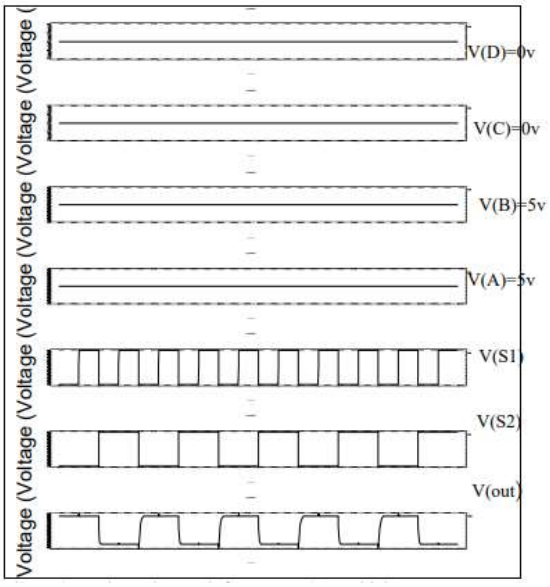

Fig IV.4.a: Schematic Result for CMOS 4:1 Multiplexer

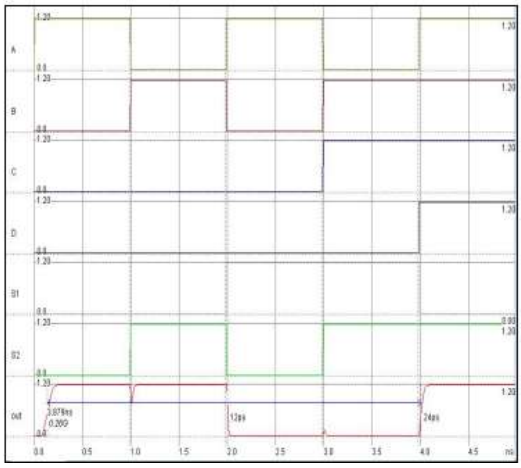

Fig IV.4.b: Layout Result for CMOS 4:1 Multiplexer

S1	S2	A	B	C	D	Out
0	0	1/0	X	X	X	A
0	1	X	1/0	X	X	B
1	0	X	X	1/0	X	C
1	1	X	X	X	1/0	D

Table IV.4.b: Truth Table for 4:1 Multiplexer

In above simulation we can see that with different control signal V(S1),V(S2) value we obtain different output,i.e.when V(S1)=V(S2)=0, V(A) is selected and so on different values are selected respectively [7].

V. APPLICATIONS

1) A barrel shifter is used in floating-point arithmetic hardware.

2) A barrel shifter is a combinational logic circuit with n data inputs,n data outputs, and a set of control inputs that specify how to shift the data between input and output [9].

3) A barrel shifter that is part of a microprocessor CPU can typically specify the direction of shift (left or right), the type of shift (circular, arithmetic, or logical), and the amount of shift (typically 1 to n-1 bits, but sometimes 1 to n bits) [12].

4) Barrel Shifter was used in processors till Pentium 3.The Athlon and K5 and Pentium-III uses Barrel Shifter [5].

VI. CONCLUSION

All of the above designed modules form an integral part of the Barrel Shifter design. By using all these circuits, 4–bit and 8–bit Barrel Shifter can be designed. The 2:1 MUX is designed for storing the falling bits and the 4:1 MUX is used for the arithmetic & logical shifting and rotating purposes.

VII. REFERENCE

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