

Design of An Active element-based Class-J Power Amplifier for 5G Wireless Communication Applications

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Abstract

This paper presents the analysis and design of an active element-based class-J Power Amplifier (PA). A proper PA needs to be designed to achieve the required power output over a bandwidth (BW) that supports the emerging 5G applications without sacrificing linearity. Among different PAs, class-J mode PA will be more suitable for linear and broadband applications. Therefore, a class-J PA design that operates at 5GHz (i.e., sub-6GHz 5G frequency band) with an active element-based approach using Silterra 130nm CMOS process technology to estimate its feasibility for integration without compromising on the performance is described in this paper. The simulation results show that the saturated power output (P_{sat}) of 27dBm with a maximum value of 13.73dB power gain and power output at 1dB compression point (P_{1dB}) of 26.2dBm are obtained with a BW of approximately 500 MHz by supplying the PA with 5V to deliver into 50 Ω load. The PA's layout with the estimated chip size of (13.8X20.0) μm^2 reveals its feasibility for the integration.

Keywords: 5G, Sub-6GHz, Class-J, Power Amplifier, OMN

Introduction

The most key building block of emerging 5G [1-3] wireless communication systems is PA, as its performance has a crucial impact on the overall system's energy consumption and BW enhancement. Among various PA modes reported in the literature [4-12], the class-J PA proposed by Steve C. Cripps in 2006 [11] has proved its potentiality and suitability for linear and broadband applications. Because of class-J PA's good wideband and linear performance it has been analysed and designed by many research scholars for different applications [13-17]. However, to achieve the required power output over desired BW of 5G applications, this class-J PA design with a tuneable inductor or capacitor-based dynamic Output Matching Network (OMN) is preferred [18]. Because, transistor's non-linear parasitic parameters that operates in class-J PA, changes the value its optimum impedance under different frequencies which directly varies the impedance value of OMN. Moreover, the emerging 5G technology need to support the higher data rates in applications such as the 5G smart meter/grid [19]. Therefore, proper OMN is becoming crucial to make this well-established class-J PA suitable for such 5G applications. In this work, the optimum impedance needed for class-J PA is calculated using

extensive waveform engineering instead of load-pull simulations, then to match this optimum impedance with the load resistance (R_L), an OMN with π -type structure is designed with an idea to replace its passive inductor with tuneable active inductor [20]. Finally, to check the PA circuit's feasibility for integration via its chip size estimation, all its passive components are replaced by active elements without affecting its performance. The class-J PA's theory is analysed in Section II. In Section-III the analysis and calculation of optimum impedance is described. The π -type OMN design to achieve class-J operation is elaborated in Section-IV. In Section-V the simulation results of the designed PA and their comparison with recent similar PA designs are discussed. In Section-VI this work's summary is briefed as conclusion.

Theory and Analysis of Class-J Pa

Based on the class-J PA's theory, with the class-B biasing point the transistor's drain current (I_D) is expressed as shown in equation (1).

$$I_D | j(\theta) = \frac{I_{max}}{\pi} + \frac{I_{max}}{2 \cos(\theta)} + \frac{2I_{max}}{3\pi \cos(2\theta)} \quad (1)$$

I_{max} is the transistor's maximum ID.

The voltage at the drain of the transistor (V_{DS}) expressed in equation (2) is obtained by presenting it with an inductive fundamental load and a capacitive second harmonic load.

$$V_{DS} | j = V_{th} + (V_{DD} - V_{th})(1 - \cos \theta)(1 + \alpha \sin \theta) \quad (2)$$

V_{DD} and V_{th} are the transistor's supply and threshold voltages.

The theoretical optimum impedances required for class-J operation mode are extracted from equations (1) & (2), can be expressed as shown in equations (3) & (4).

$$Z_{f0} = \frac{(V_{DD} - V_{th})(1 + j\alpha)}{I_{max}/2} = R_{opt} + j\alpha R_{opt} \quad (3)$$

$$Z_{2f0} = -\frac{(V_{DD} - V_{th})j\alpha}{2\left(\frac{2I_{max}}{3\pi}\right)} = -\frac{j3\pi}{8} \alpha R_{opt} \quad (4)$$

Equation (5) represents the transistor's optimum resistance

$$R_{opt} = 2(V_{DD} - V_{th}) \div I_{max} \quad (5)$$

By presenting these Z_{f0} & Z_{2f0} to the transistor a boost in the drain voltage (V_{DS}) with some phase shift that reduces overlap between V_{DS} and I_D , can be observed as shown in Figure 1, making the class-J PA more efficient.

In addition, due to its non-switching operation mode this class-J PA's linearity will be same as class-B or AB PAs, although the V_{DS} and I_D waveforms in Figure 1 resemble the switching mode PA's waveforms. This class-J PA will be more suitable for wideband applications as it will not use any harmonic traps like class-B PA.

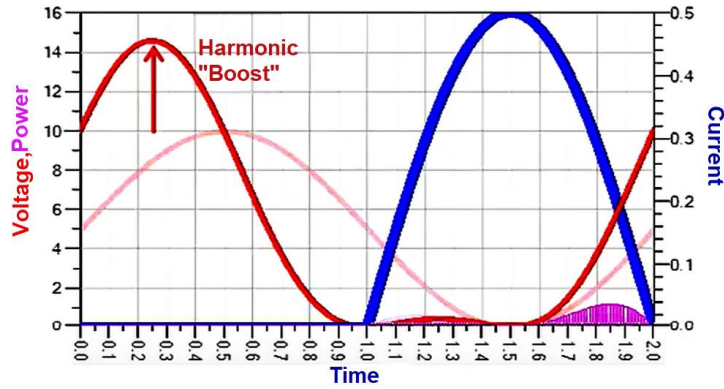


Figure 1. The V_{DS} and I_D of class-J PA's transistor

Optimum Impedance Analysis

The values of optimum impedances (Z_{f0} & Z_{2f0}) required for class-J PA operation are theoretically calculated from the V_{DS} and I_D expressions as shown in equations (3) & (4) in terms of R_{opt} . But in practice, these optimum impedance values will deviate from their theoretical values because of the transistor's non-linear capacitance variation with frequency and power output. Therefore, generally, these practical optimum impedance values can be determined with the help of load-pull simulations at different frequencies and power outputs.

There is no possibility to perform load-pull simulations for the PA design in the Mentor Graphics (MG) EDA tool used, therefore a reference R_{opt} value has been initially chosen. To obtain this reference R_{opt} value, the aspect ratio of the selected transistor is altered accordingly, because this R_{opt} value depends on its transistor's maximum drain current (I_{max}), which can be changed by its (W/L) ratio and the biasing voltages.

Therefore, in this work, a 130nm Silterra nm_hp transistor (M1) has been chosen to get the reference R_{opt} value of 4.3Ω . To calculate the theoretical value of I_{max} corresponding to the reference R_{opt} value using equation (5), the V_{DD} and V_{th} values must be known. The value of V_{DD} has been chosen as 5V to allow for the maximum swing across the selected transistor M1. The V_{th} value of the transistor M1 is extracted from its transconductance (gm). The value of gm is obtained by differentiating the I_D concerning V_{GS} (i.e., dI_D/dV_{GS}), and then this gm value is differentiated concerning V_{GS} (i.e., dgm/dV_{GS}) with the use of EZ waveform calculator utility of the EDA tool to extract the V_{th} value. The V_{GS} value where the derivative of gm with respect to V_{GS} is maximum is taken as the transistor's V_{th} value (i.e., $V_{th} \cong 0.5V$), as shown in Figure 2.

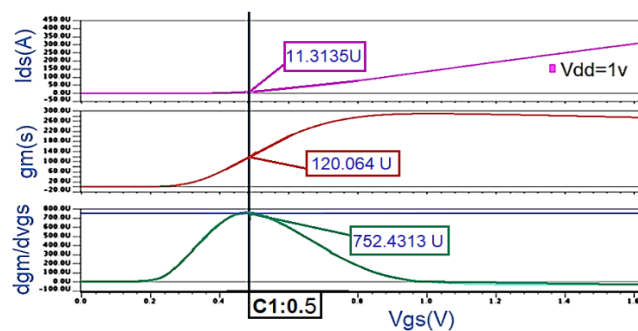


Figure 2. V_{th} value of nm-hp transistor

With these V_{DD} and V_{th} values, the theoretical I_{max} value calculated using equation (5) is 2.1A for corresponding reference R_{opt} value 4.3 Ω , and the theoretical optimum impedance values are obtained by substituting this R_{opt} value in equations (3) & (4).

To validate this theoretical optimum impedance value, the width (W) of the transistor (M1) is altered as (2x5 μ m) and is supplied with the bias voltages of $V_{DD} = 5V$, $V_{GS} \cong V_{th} \cong 0.5V$. Corresponding to these bias voltages and transistor's size, the I_{max} value of 2.1A is obtained, leading to a R_{opt} value of approximately 4.5 Ω . This R_{opt} value is calculated with the help of EZ waveform calculator utility, as shown in Figure 3, is almost equal to its theoretical value.

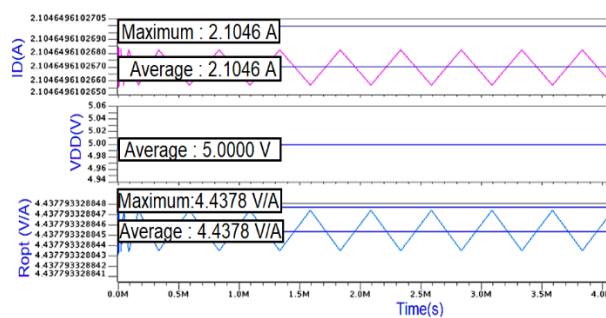


Figure 3. R_{opt} obtained from EZ waveform calculator

As another approach, the transistor (M1)'s R_{opt} value can be determined by calculating its output impedance (Z_{out}) in terms of S-parameters with the help of .extract and .defwave commands in the command window by conducting SST analysis at 5GHz frequency as shown in Figure 4.

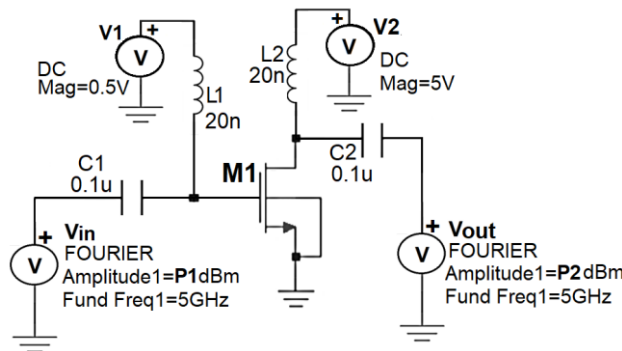


Figure 4. Extraction Z_{out} of the transistor (M1) from S-Parameters at 5GHz frequency

The class-J PA mode operation of the transistor can be achieved by matching its determined R_{opt} value of optimum impedances (Z_{f0} & Z_{2f0}) with the load/output port resistance (R_L) using a proper OMN design.

1. Design of Π -Type OMN

A proper OMN design is the key to achieving class-J PA operation. Generally, the class-J PA's wideband operation can be achieved using different matching methods such as lumped passive element-based L, π , T-type networks or transmission lines based distributed networks. However, the transmission line based distributed OMN design may occupy a larger area which leads to an increase in the cost of integration, whereas the passive lumped-element based higher-order OMN design with a minimum of two inductors may reduce the power output and

efficiency due to the integrated inductor's losses used while implementing the PA circuit.

Therefore, initially the OMN using passive element-based π -structure with 2 capacitors and 1 inductor, as shown in Figure 5, has been chosen with an idea to replace its lumped inductor with an active inductor after achieving the PA's desired performance metrics.

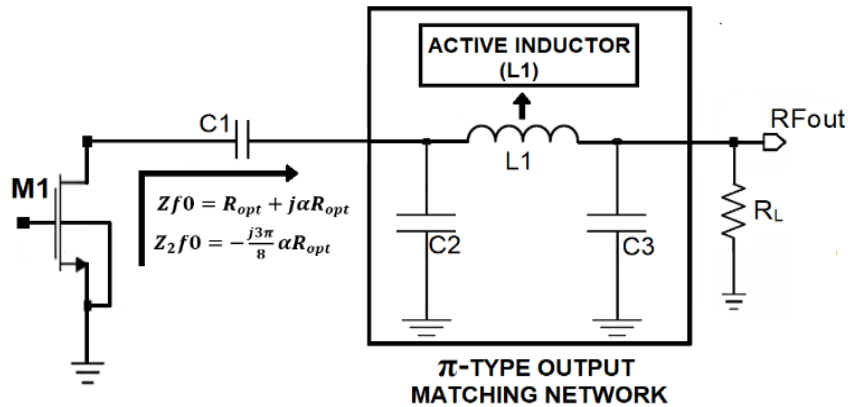


Figure 5. π -type OMN design for class-J PA

As the class-J PA of this work is planned to design at a centre frequency of 5GHz (i.e., sub-6GHz 5G frequency), its desired BW can be obtained by designing the OMN in terms of its Quality factor that will be represented as ($Q=f/BW$). Therefore, this π -type OMN with two back-to-back connected L-sections is designed by choosing a Q value of 10 to achieve desired BW of approximately 500MHz to make the PA appealing for wideband 5G applications.

Simulation Results And Discussion

The designed PA's performance with π -type OMN is validated by performing its schematic circuit simulations using the MG EDA tool. To achieve the class-J PA operation, the transistor (M1)'s drain is biased with voltage $V_{DD} = 5V$, the gate is biased with voltage $V_{GS} \cong V_{th} \cong 0.5V$ (i.e., class-B bias point) and stabilized across desired frequency range using a simple RC circuit. The class-J PA's schematic circuit with its π -type OMN is shown in Figure 6.

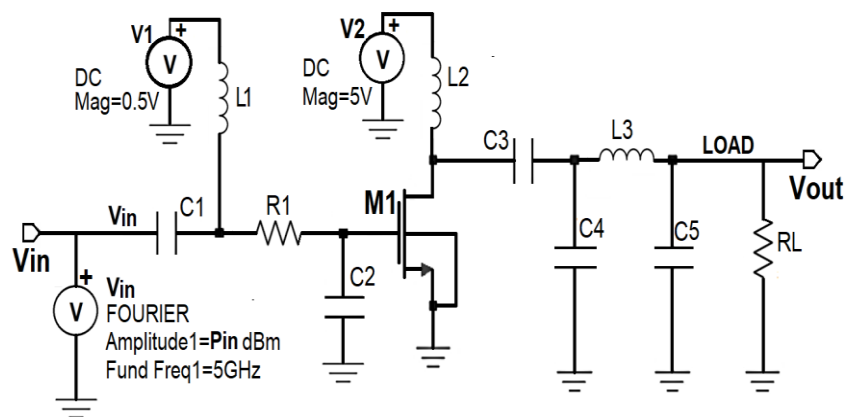


Figure 6. Schematic class-J PA circuit with

$$(R_{opt} \cong Ref R_{opt}) \text{ and } (R_{opt} \cong Z_{out})$$

The component values of schematic class-J PA circuit whose OMNs designed corresponding to value of R_{opt} calculated using EZ waveform calculator (i.e., $R_{opt} \cong Ref R_{opt}$) and R_{opt} value equal Z_{out} of the transistor (M1) which is obtained in terms of S-parameters (i.e., $R_{opt} \cong Z_{out}$) are shown in the Table-1.

Table -1: Component values of Figure 6

Components	Values corresponding to OMNs with	
	$(R_{opt} \cong Ref R_{opt})$	$(R_{opt} \cong Z_{out})$
C1=C3	0.1uF	0.1uF
C2	5pF	5pF
C4	5.2pF	16.5pF
C5	2.6pF	6.4pF
L1=L2	20nH	20nH
L3	0.45nH	0.2nH
R1	10Ω	10Ω
RL	50Ω	50Ω

Then, this designed class-J PA is supplied with 1-Tone Continuous Wave (CW) RF input signal with a centre frequency of 5GHz to evaluate its performance. The important performance parameter waveforms of the simulated PA are obtained by typing their mathematical expressions in command window while performing SST analysis corresponding to the power input (Pin) sweep of Fourier RF input source as shown in Figure 7. It is noticed that the PA delivers 11 dB maximum power gain and 26 dBm P_{sat} value.

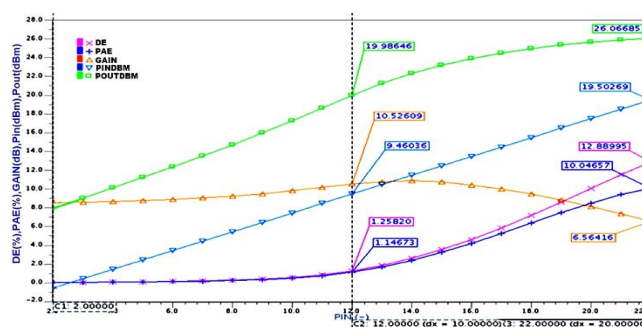


Figure 7. The class-J PA's performance parameters with $(R_{opt} \cong Ref R_{opt})$

Similarly, the class-J PA's performance parameters with its π -type OMN designed corresponding to the, R_{opt} value equal Z_{out} of the transistor (M1) which is obtained in terms of S-parameters (i.e., $R_{opt} \cong Z_{out}$) are shown in Figure 8.

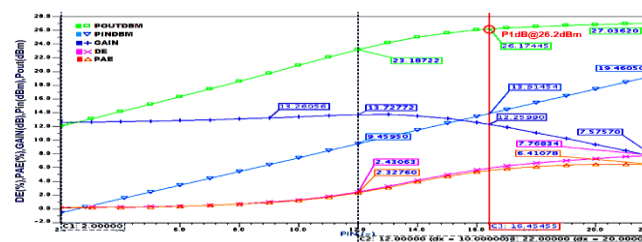


Figure 8. The class-J PA's performance parameters with $(R_{opt} \cong Z_{out})$

It is noticed that when this PA is supplied with the same 1-Tone CW RF input signal at 5GHz centre frequency, the PA delivers a P_{sat} value of 27dBm and 13.73dB maximum power

gain for a BW approximately 500 MHz corresponding to the Q factor value chosen. In addition, the PA's linearity is measured using a 1dB compression point (P1dB). The Pout delivered at P1dB is 26.2dBm which is almost equal to P_{sat} , it represents that the PA is exhibiting good linearity.

Post validation of PA's performance parameters its layout is designed for the chip size estimation. As this PA is initially designed using lumped passive components, not only the lumped inductor of π -type OMN, all other passive components of the PA also replaced by active elements (transistors) as shown in Figure 9.

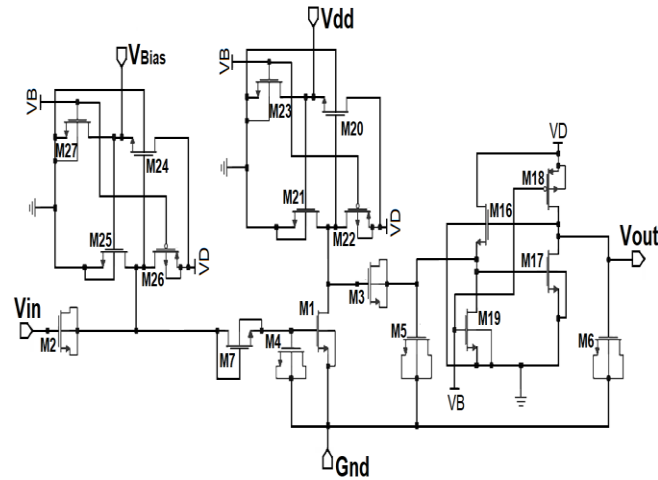


Figure 9. Active element-based schematic circuit for layout design of class-J PA

The designed class-J PA layout simulation has been carried out using MG EDA tool. The optimization and arrangement of transistors was made to reduce its chip area. The estimated chip layout size of this active element-based class-J PA is (13.8 X 20.0) μm^2 as shown in Figure 10.

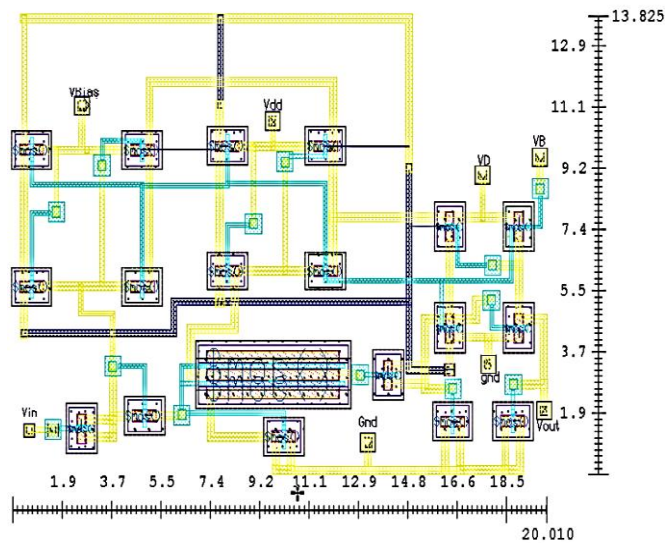


Figure 10. The core layout of class-J PA (13.8 X 20.0) μm^2

This class-J PA's performance parameter comparison with similar recently published PAs is shown in Table-2.

Table-2. class-J PA's Performance comparison

Reference	This work	[24] 2021	[23] 2020	[22] 2018	[21] 2017
Technology	CMOS	CMOS	GaN	GaN	CMOS
Class	J	J	J	J	J
Stage	Single	Two	Single	Single	Two
Frequency[GHz]	5	9.5	3.2	3	28
BW [GHz]	4.8-5.3	8.7-11.8	2.5-3.8	2.5-3.5	22-34
P1dB[dBm]	26.2	18	-	-	-
Psat [dBm]	27	20	42	40	16.2
Max Gain [dB]	13.73	15	13.3	10	15

The class-J PA designs shown in Table-2 were used different technologies and frequencies, hence their comparison is bit difficult. Irrespective of the difficulty in comparison, it is worth noting that a 28GHz two-stage class-J PA design using 28nm CMOS technology reported in [21] delivers a 15dB power gain and 16.2 dBm P_{sat} , whereas our single-stage class-J PA delivers 13.73 dB maximum power gain and 27 dBm P_{sat} . A class-J PA design with high power GaN transistor in [22] delivers 10 dB maximum power gain and 40 dBm P_{sat} , whereas our class-J PA with 130nm Silterra transistor delivers 13.73 dB maximum power gain with 27dBm P_{sat} along with 26.2 dBm Pout at P1dB which is almost equal to P_{sat} represents its good linearity. A class-J PA with a novel OMN synthesis technique for presented in [23] delivers a P_{sat} of 42dBm with 13dB power gain and good efficiency over broadband using 10W GaN transistor, although our PA design uses a 130nm Silterra transistor it delivers a 13.73 dB maximum power gain. A 130nm CMOS class-J PA that delivers 20.2 dBm P_{sat} with 15 dB maximum power gain using two-stage structure is reported in [24], however our PA design 13.73dB maximum power gain using single-stage. Although, our class-J PA design delivers the good power gain with linearity and exhibits its feasibility for integration, the remaining PA's performance metrics like BW and efficiency can be further improved to implement it in emerging wideband 5G applications.

Conclusion

Initially in this paper, the selected transistor's optimum impedance (R_{opt}) value is analysed and determined using waveform engineering and by calculating the Z_{out} of the transistor from its S-parameters, which is needed to achieve class-J PA operation. Finally, a class-J PA with π -type OMN that matches the determined optimum impedance with a load impedance of output port is designed, which delivers a P_{sat} of 27dBm with a maximum value of 13.73dB power gain over a BW of approximately 500MHz. The P1dB of PA is almost nearer to its P_{sat} value, revealing that it can provide good linearity. In addition, this active-element-based class-J PA's layout reveals that it is feasible for integration. However, the enhancement work of this PA's other performance metrics like BW and efficiency is in progress to improve its suitability for (sub- 6GHz) 5G wideband applications.

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2. Competing Interests

No competing interests were disclosed.

3. Data availability

No data is associated with this manuscript.

4. Grant Information

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