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A Novel Design of CMOS Limiting Amplifier

By

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Abstract

Communication system is used in RF and microwave, LAN's, mobile phones, base station monitoring, surveillance, satellite communications, transmitter antenna and receiver antenna testing. A multi-stage limiting amplifier & Frequency Modulation or Frequency Shift Keying demodulator is used in a 455-kHz signal processor. On chip feed forward offset cancellation circuit uses limiting amplifier. A quadrature detector is used in the Frequency Modulation or Frequency Shift Keying demodulator, & detector is consist of phase built into the chip and a tank phase shifter external to the chip. Image Frequency signal processor consumes milli Watts, 2-V power supply, and sensitivity about 72 dBm with demodulation constants of 20 milli Volts / kilo Hz and 10-kHz deviation. The active area is 0.2 mm2 and it uses 0.3- micron digital Complementary MOS technology. Limiting amplifier used in communication system and wireless communication

Index Terms—Complementary MOS IC, Analog and Digital de-modulators, Image Frequency signal processing, Quadrature Detector and Limiting Amplifier.

Introduction

The Complementary MOS 455-kilo Hertz signal processor designed for super heterodyne communication systems is in Fig. 1 shown. It have 2 functions, they are magnitude control and Frequency Modulation or Frequency Shift Keying demodulation. In Frequency Modulation or Frequency Shift Keying applications the limiting amplifier selected as a magnitude control. In this case, the DC offset reduces the sensitivity, which consequently degrades BER recovery. At each gain stage, feed forward offset cancellation technology is implemented, which demonstrates instantaneous response and high-level integration compared to conventional external passive approaches [1].

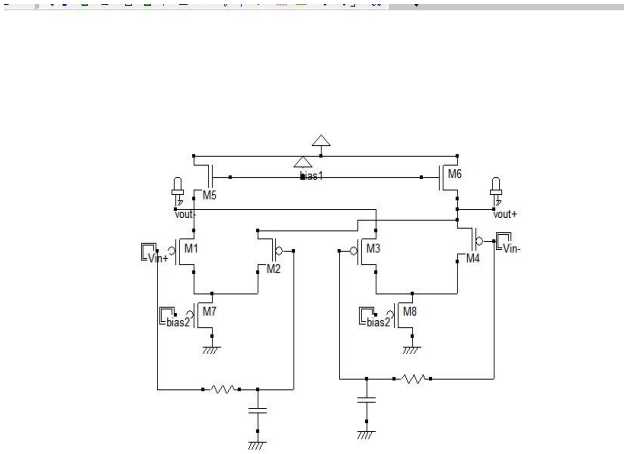
Frequency-shift keying (FSK) is a discrete FM signal that may be dealt with as such Frequency Shift Keying frequencies are spread out and arranged on a nominal service frequency. The FSK or 4-FSK BW is lesser and Frequency Modulation/Frequency Shift Keying demodulator have strong frequency discrimination. The Quadrature detector is have FM/FSK demodulator. It consisting eexternal tank phase shift network and integrated phase detector for low voltage operation.

Hardware Design

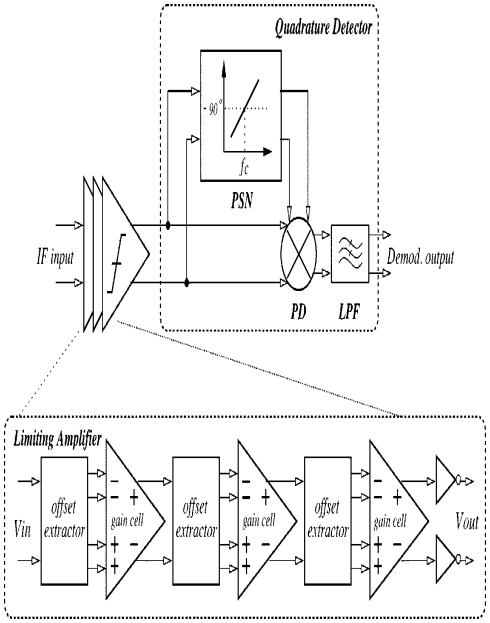
Limiting Amplifier

It have various stages of input magnitudes in an amplifier chain. Input active range should be in a pager application, this amplifier chain must produce a tiny signal gain is not less than 70 dB. It must produce a high-pass function in order to compensate for mean amplitude displacement from zero caused by mismatch. To lessen the AM–PM conversion effect, the top BW is 10 times of the IF [3], 10 kHz selected at bottom. It has no effect at 455 kHz [4] of data band. As illustrated in Fig. 1, the suggested limiting amplifier has three levels of gain cells. In three cells first and second cell are similar and third has an auxiliary output driver built in. This architecture uses a feed forward offset cancellation technique rather than the traditional negative feedback method [5].

The amplifier's core is made up of cross-connected source-coupled pairs with differential input pairs. The previous stage is connected to all of these source-coupled pairs. In addition, the offset extraction circuit is implemented as an RC network at each pair's input. When $f_{in} > RC\ f_{cutoff}$, then traditional source coupled pair is equal to circuit topology. When the f_{in} is lower than the RC f_{cutoff}, on the other hand, the offset voltage is higher. As a result, the input common-mode voltages of the two source-coupled pairs diverge. The amplifier reject the offset voltage equipped and supplied at input due to the move-connected mechanism and cross connected mechanism. Offset generated within the cutting-edge level may be cancelled within the subsequent degree and cancelled the offset generated in current stage. Because each step's offset extractor circuit nearby wishes to cutting the offset voltage caused through the prior degree and offers an immediate response. As a result, each gain cell uses the lesser R and C. In conventional digital CMOS technology, triode biased pMOS resistor and pMOS gate to bulk capacitor is used for getting the offset extractor's long time constant RC network. Whilst the pMOS is in accumulation mode, the gate to bulk capacitance is 2 to 3pF.



Offset Extractor



Architecture and Gain

The created high-pass function's 3-dB corner frequency is 10 kHz. The offset causing CMOS process fluctuation cover the planned offset cancellation range is in 230 mV. The source coupled pair output impedance and accompanying parasitic capacitance, govern the gain stage's high-frequency roll-off, as shown in (1).

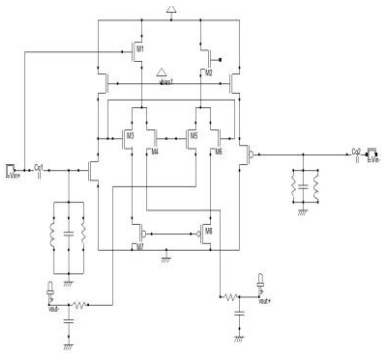
$$f_{-3\,\mathrm{dB}} = \frac{1}{2\pi(r_{o1}//r_{o5}//r_{o3})\cdot(C_{gd5}+C_{gd1}+C_{gd3})}. \quad (1)$$

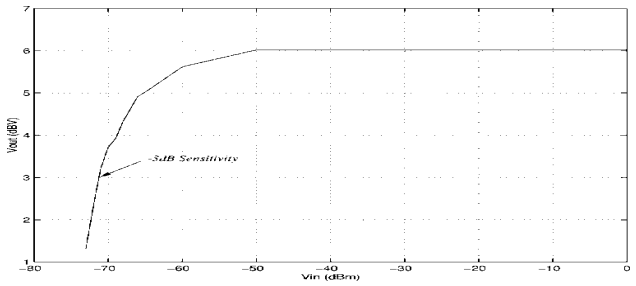
A three-stage topology is chosen, taking into account the balance between BW, gain, and usage of power. The first two identical stages have a 4.6-MHz bandwidth and a 28-dB differential voltage gain. The last stage includes the addition of two supplementary output drivers.

Quadrature Detector

FM/FSK demodulation used by quadrature detector. PSN shifts the phase that is proportional to f_{inst} . The difference between original FM and phase shifted signal detected by the phase detector. Finally, low pass filter is used to recover the demodulated output and remove the high-frequency noise. The frequency deviation is converted into phase shifting. The phase-shift network response is given by Equation (2), where is the incoming FM signal by an amount that is proportional to its instantaneous frequency. The phase difference between the original FM signal and the phase-shifted signal is then detected using a phase detector (PD). Finally, the low pass filter is used to remove high frequency noise and recover the demodulated. The frequency deviation is converted into phase shifting. In the phase-shift network phase response of the carrier frequency a proportional constant. So a good phase shift value can help with frequency discrimination in demodulation.

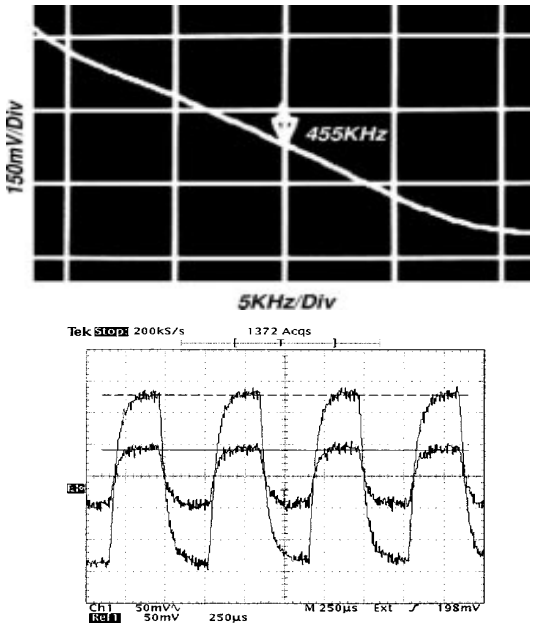
$$\phi(f) = \frac{\pi}{2} + 2\pi K(f - f_o).$$





Sensitivity

A differentia- tive circuit structure used for quadrature detector. In the phase shifting network have the external tank circuits with $Q = 20$ & quadrature capacitors are assembled on chip. At IF signal band, a linear phase shift gives as output. Gilbert type phase detector is used to detect the difference between the output of limiting amplifier and output waveform of the phase shift network. The upper and lower pMOS devices are connected to the output of phase shift network, function as commuting switches. For low supply voltage & good linearity no tail current source is working in phase detector [6]. First order external low pass filter used to remove the high frequency harmonics. The modulating signal's frequency variation is proportional to demodulated signal amplitude at the filter output.



Vout versus input frequency deviation
FSK output levels

In spite of that all the data is single ended, the four levels are separated by more than 70 millivolts.

Experimental Results

Technology	0.6micro m CMOS
Limiting Amplifier	
Single stage gain	28dB
Single Stage bandwidth	4.6 MHz
-3dB sensitivity	-72 dBm @50 ohm
Demodulation Constant	20 mV/KHz
Max. freq deviation	+ or – 10 KHz
Output LSB for 4 FSK signal and supply voltage	70 mv and 2 V
Power Consumption	2.3mW

0.6 m single poly double metal digital CMOS technology used in IF 455-kHz signal processor. From a single 2 Volts power supply, the whole circuits draw 1.15 mA. The circuits can work with a low supply voltage of 1.8 V. Each stage have limiting amplifier's gain stages each have a gain of 28 dB and a 4.6 MHz bandwidth. When the input impedance matches 50, the 3 dB sensitivity input level is 72 dBm.

At IF 455 kHz, quadrature detector's demodulation constant is 20 mV/kHz, as shown in Fig. 6. The rang of the FM deviation can extend well beyond 20 kilo Hz. The 4 levels are separated by more than 70 milli V, despite the fact that all of the data in this paper is single ended.

Conclusion

The feed forward offset cancellation is used by limiting amplifier, it consumes less than 0.5 mA at each of the three gain stages. This limiting amplifier's sensitivity is 72 dBm. Each gain cell's passive offset-extraction network is included on same chip. The quadrature detector is made up of an external tank phase shifting network and an on-chip phase detector, is utilized in the FM/FSK demodulator. The demodulator runs on less than 0.7 mA and processes a high demodulation constant of 20 mV/kHz.

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