ANALYZING THE DESIGN OF NANOSCALE USING FINFET BASED SRAM CELL TO LEAKAGE POWER REDUCTION

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Abstract:-

Short channel effects and other parameter modifications have a significant influence on semiconductor devices at nanoscale technology nodes. To ensure sufficient manufacturing yield while balancing power, area, and resilience, a creative and comprehensive circuit-level technique is needed. A different approach to bulk devices for lowering leakage power and short channel effects is FinFET-based design.

Numerous strategies were previously used to reduce leakage power, but they were only able to do so to a limited extent. I've developed a hybrid method and applied it to a 6T SRAM cell with a FinFET foundation. Because leakage current is reduced and there is no area penalty, it lowers power dissipation in standby mode. At a fixed 45 nm channel length on Cadence Virtuoso at room temperature, we achieved a decrease in leakage current and static power dissipation at 25.59% and 31.29%, respectively, compared to the standard FinFET.

Keyword:-

Leakage power, SRAM (Static Random Access Memory) , Hybrid, AVL (Adaptive Voltage Level), Leakage current, MTCMOS(Multi-threshold voltage complementary metal-oxide semiconductor)

1.) Introduction:-

Large, high-performance memories, such as static random-access memory (SRAM), are becoming increasingly necessary due to the growing need for multimedia-rich applications, such as those found in portable and handheld devices. The on-die cache memory takes up a significant amount of the chip's overall silicon area. It also has a big impact on the multimedia application's total power use.

The CMOS devices' ability to scale continuously allows for high package densities, which contribute to a reduction in the total Si area [1]. The first design element that the designer community adores is the supply voltage (VDD) decrease, which helps to reduce total power consumption.

Although the power consumption is appreciated, there are two significant issues raised by this reduction in VDD: data stability and leakage power. Almost 40% of the power consumed by today's high-performance chips comes from leakage current.

Statistical dopant fluctuations, oxide thickness variations, and line-edge roughness increase the spread in transistor threshold voltage (Vth) and consequently the on- and off-currents when MOSFETs are scaled down to the nanoscale regime. Future technologies will see a fall in threshold voltage, which will result in very high power consumption from memory devices. Therefore, power consumption is the main issue with the next generation of SRAM cells. For better scalability, the FinFET transistor structure has been created as an alternative to the bulk-Si MOSFET structure [2]. The channel/body is a Si fin, not a flat Si surface, and the gate electrode is straddled by the fin. Effective channel width is represented by the fin height, while effective body thickness is represented by the fin width. When the Si fin is in the on state, current travels down the gated sidewall surfaces between the source and drain. The use of a thin body, that is, by making the fin extremely small, less than the channel length, suppresses short-channel effects (SCE).

2. Background AND Analysis:-

Optimizing the device structure is crucial for designing dependable and low-power SRAM cells using 45 nm FinFET technology. Strong FinFET-based SRAM cell architecture at 45 nm technology should ensure minimal parameter variation sensitivity, correct operation, and low leakage power [2]. Additionally, we examine the effects of changing the width of access, load, and driver FinFET transistors on static power and leakage current. Using the Cadence Virtuoso simulation tool, all evaluations for the static leakage power of the FinFET-based SRAM cell have been completed. The DG-FinFET device construction is depicted in Figure 1.

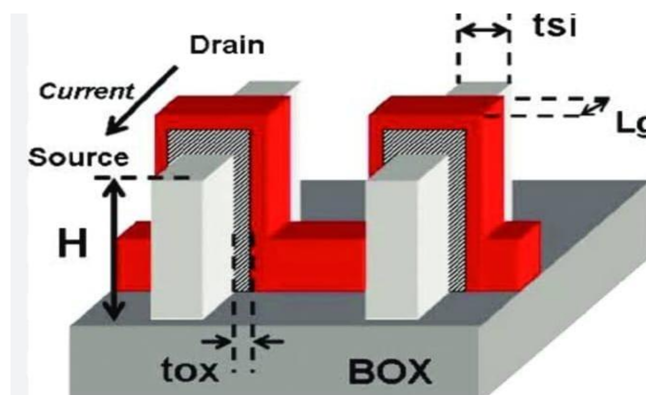

Fig 1: Double gate FinFET Structure

Because of its low parameter fluctuation and ability to reduce numerous short channel effects, the FinFET device is the most popular contender at sub 45 nm technology. FinFET is used to develop a variety of nanoscale memory circuits that must accept environmental conditions and

have low power dissipation. FinFET-based SRAM cells also have higher noise margins and faster switching rates.

The design of Bulk MOSFET memory cells at a 45 nm node is complicated by the heightened short channel effects (SCE) and parameter sensitivity. It is well known that a FinFET device's size has an impact on the memory circuit's power dissipation and performance [3]. For this reason, designing an efficient circuit is exceedingly challenging. Transistors based on DG-FinFETs with shorted gate terminals are used to build all of the circuits.

Two cross coupled inverters, sometimes known as latches, and two access FinFET transistors are the components of the 6T SRAM cell, as seen in Figure 2. Each bit in an SRAM is stored on the four FinFETs (M3, M4, M5, and M6) found in the two cross-coupled inverters. Bit line (BL) and bit line bar (BLB) are linked to the source terminals of both access FinFET (M1 and M2). Bit lines are segregated from latch and access FinFET are turned off when the word line is low. If the voltages stay at VDD and VSS in this situation, the latch can hold the bit. Bit lines (BL and BLB) are linked to the latch and access FinFET are ON when the word line is high. Data transmission for both write and read operations is the purpose of these bit lines [2]. Three types of operation are available for SRAM cells: Write mode: This mode allows the original bit value of an SRAM cell to be replaced with a different bit value. Hold mode, often known as data retention, allows the SRAM cell to store data indefinitely as long as it is powered. The SRAM cell can convey its stored data while it is in read mode. The data is not impacted by this method of operation:--

A).Write operation:- Pulling the word line high (WL=1) is necessary to activate the access transistors(M1 and M2 (in order to carry out the write operation .We can now carry out the write operation. Bit line (BL) receives the essential data to be written, while bit line bar (BLB) receives its complement. The cell would then adjust its state in accordance with this. The necessary data is sent to the cell when the latch state is changed, deactivating the word line (WL=0).

B). Hold operation:- The access FinFET transistors (M1 and M2) disconnect the SRAM cell from the bit line (BL) and bit line bar (BLB) if the word line is not specified (WL=0). As long as the two cross-coupled inverters made up of M3 and M6 are linked to the supply voltage (VDD), they will continue to support one another. Leakage current refers to the current flowing from the VDD in this condition.

C). Read operation:- The word line must first be asserted to high (WL=1) in order to activate the access FinFETs (M1 and M2) and access the latch in order to read the data from the output node in the SRAM cell. Currently, both bit lines (BL and BLB) are pre-charged to "1."

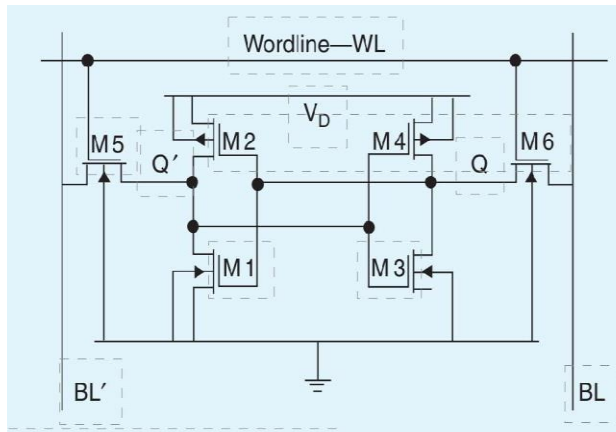

Fig 2 : FinFET Based 6T-SRAM cell

Depending on the latch's condition, one bit line will stay pre-charged and the other will be discharged to ground. At this point, the sense amplifier's inputs are receiving both bit lines. This amplifies the data to a large degree and eventually provides the information of the stored bit. Figures 3 and 4 display the leakage current and static power dissipation waveforms of the FinFET-based 6T SRAM, respectively.

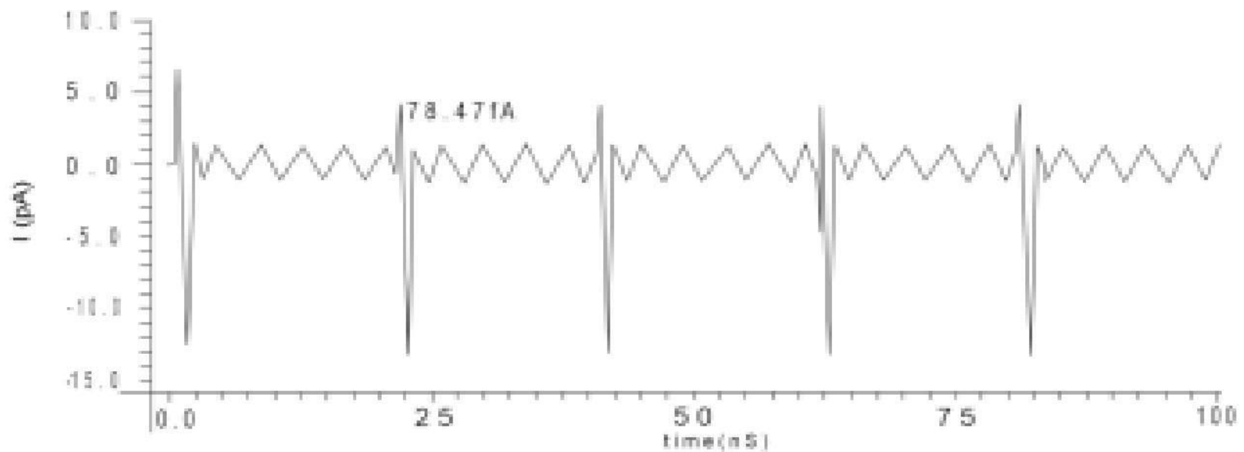

Fig 3: Leakage current of FinFET Based 6t- SRAM cell

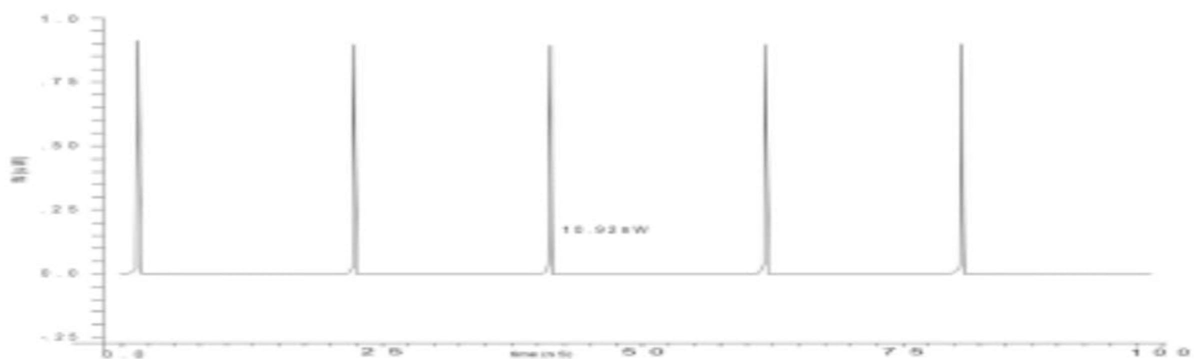

Fig 4 Static power dissipation of FinFET Based 6T SRAM Cell

3. PRIOR DESIGN TECHNIQUES FOR POWER LEAKAGE REDUCTIONS:-

A). Adaptive Voltage Level (AVL) Technique:-

Reducing gate leakage currents also seems to be particularly promising when using an Adaptive Voltage Level (AVL), which permits the application of the full supply voltage in the active mode and a lower supply voltage in the inactive mode [4].

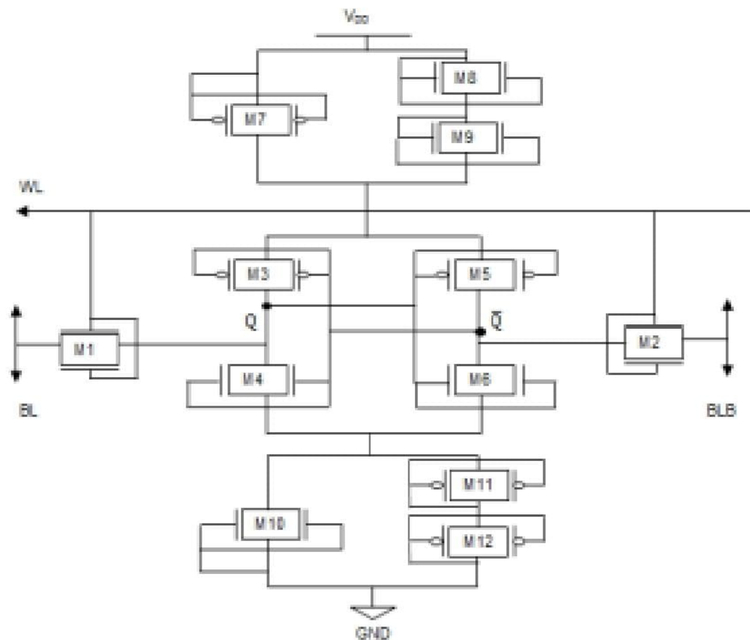

Fig 5 : Implementation of AVL technique on FinFET based 6T SRAM Cell

Gate leakage current has already been shown to be significantly reduced using an approach akin to using AVL to raise the ground potential [5,6]. Thus, the suggested SRAM cell coupled with an adaptive voltage level (AVL) circuit at either the supply node (referred to as AVLS) or the ground node (referred to as AVLG) is simulated.

In this study in order to further reduce leakage, and its leakage characteristics are examined. Together, these two circuits—referred to as AVLG (lower AVL) and AVLS (upper AVL)—provide the 6T SRAM cell based on FinFETs with less leakage. The circuit of a FinFET-based 6T SRAM cell using the AVL approach is depicted in Figure 5. Figures 6 depict the leakage current waveform of a FinFET-based 6T SRAM that was developed utilizing the AVL approach, respectively.

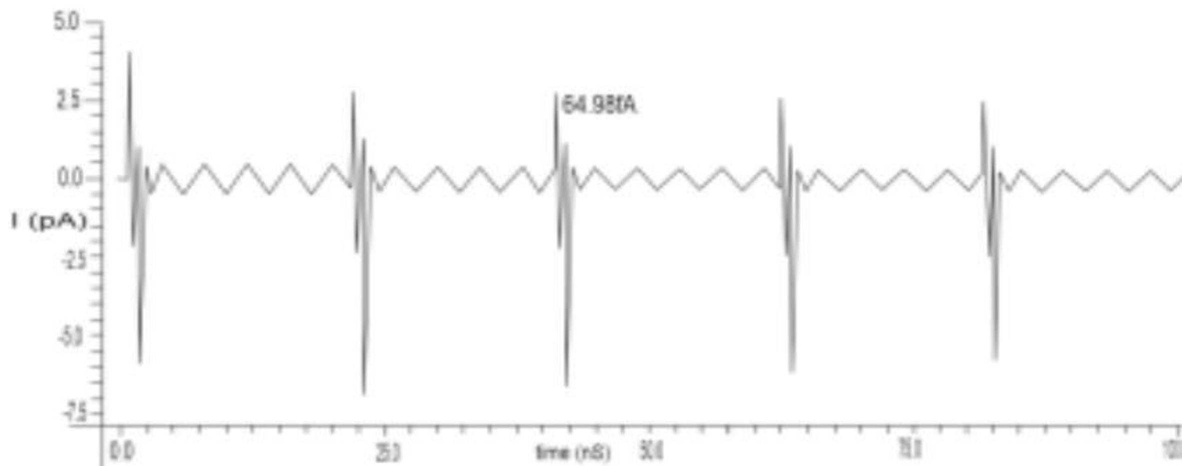

Fig 6 : Leakage current waveform by AVL technique on FinFET Based 6t SRAM Cell

B). MTCMOS Technique :-

Transistors with different threshold voltages (Vth) are used in multi-threshold CMOS chips, a variant of CMOS technology, to improve power or delay. When an inversion layer occurs at the interface between the transistor's substrate (body) and insulating layer (oxide), it is known as the MOSFET's Vth gate voltage. In order to reduce clock durations on crucial delay routes, low Vth devices switch more quickly. The trade-off is much higher static leakage power for low Vth devices. On non-critical channels, high Vth devices are utilized to cut down on static leakage power without causing a delay cost. When compared to low Vth devices, most high Vth devices minimize static leakage by a factor of ten [7].

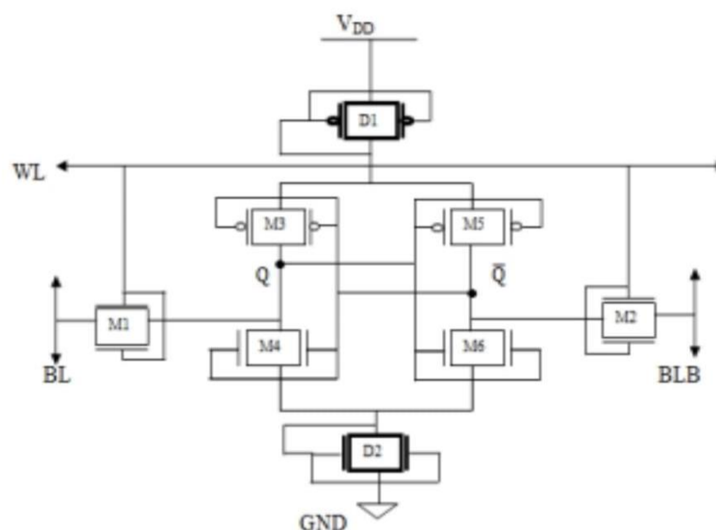

Fig 7: Implementation of MTCMOS technique on FinFET based 6T SRAM Cell

High threshold sleep transistors are used on top and bottom of the logic circuit in the MTCMOS approach to detach low threshold voltage transistors from the power source. Figure 7 illustrates the usage of transistors with low threshold voltages (low-Vth) in logic architecture. The sleep signal regulates the sleep transistors.

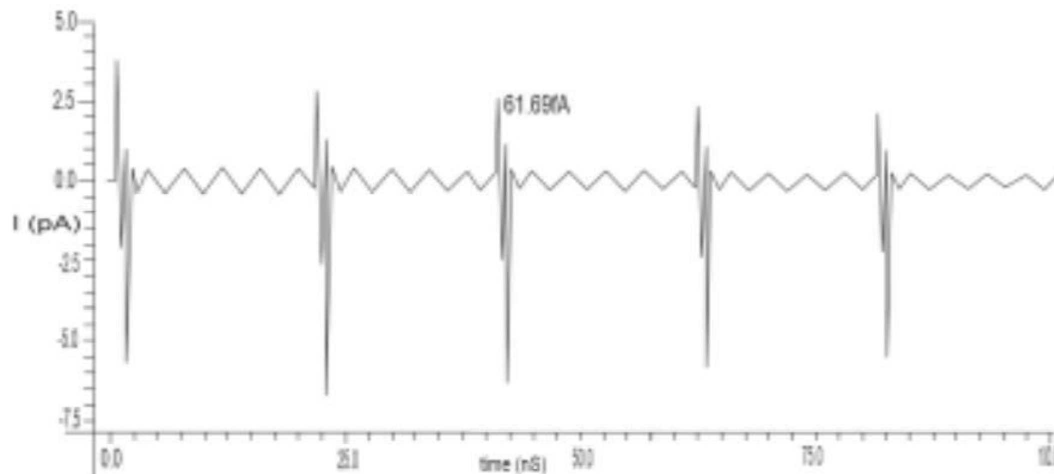

Fig 8: Leakage current waveform by MTCMOS technique on FinFET Based SRAM Cell

The low Vth logic receives a virtual power and ground from the two high Vth transistors when the sleep signal is abandoned during the active mode. The sleep signal is asserted while the circuit is in the inactive mode, which compels the two high Vth transistors to turn off and disconnect the power lines from the low Vth logic. In standby mode, this leads to a very low leakage current from power to ground [8]. Figures 8, respectively, display the leakage current waveform of a FinFET-based 6T SRAM that was constructed using the MTCMOS approach.

4. HYBRID TECHNIQUES THAT ARE PROPOSED FOR REDUCING LEAKAGE POWER:-

A high threshold transistor is employed in the hybrid SRAM cell technology, which lowers the sub threshold leakage in the SRAM cell [9]. For the 6T SRAM cell to work normally in active mode, the High Vth transistor has to be ON. To improve leakage control, the High Vth transistor has to be turned off while in standby mode. On the other hand, any transistor's threshold voltage may be altered. However, it may cause the SRAM cell's read latency to rise. As a result, PMOS transistor threshold voltage is raised. In a similar vein, increasing the oxide thickness of the pass and NMOS transistors lowers gate leakage.

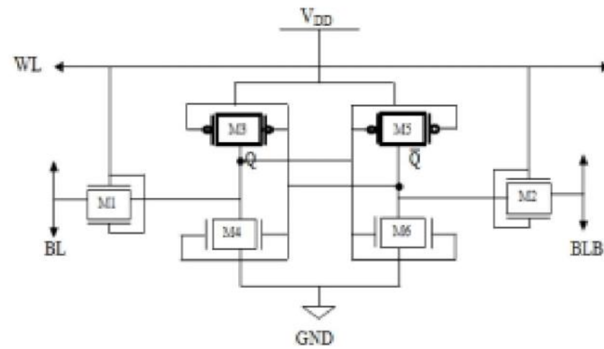

Fig 9: Implementation of Hybrid Technique on FinFET Based 6T SRAM Cell

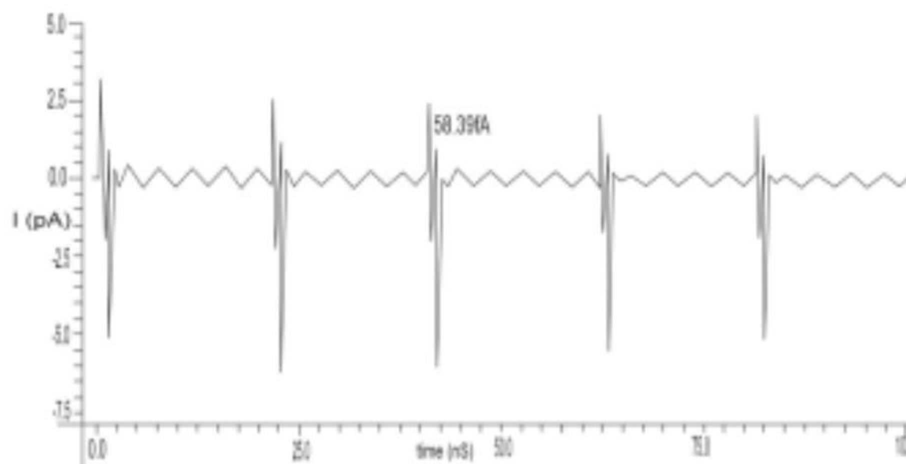

Fig 10: Leakage current waveform by Hybrid technique on FinFET Based SRAM Cell

Figure 9 illustrates the circuit of a 6T SRAM cell based on FinFETs using the hybrid approach. Figures 10 and 11, respectively, depict the output waveforms for the FinFET-based 6T SRAM cells that were implemented utilizing the hybrid approach in terms of leakage current and static power dissipation.

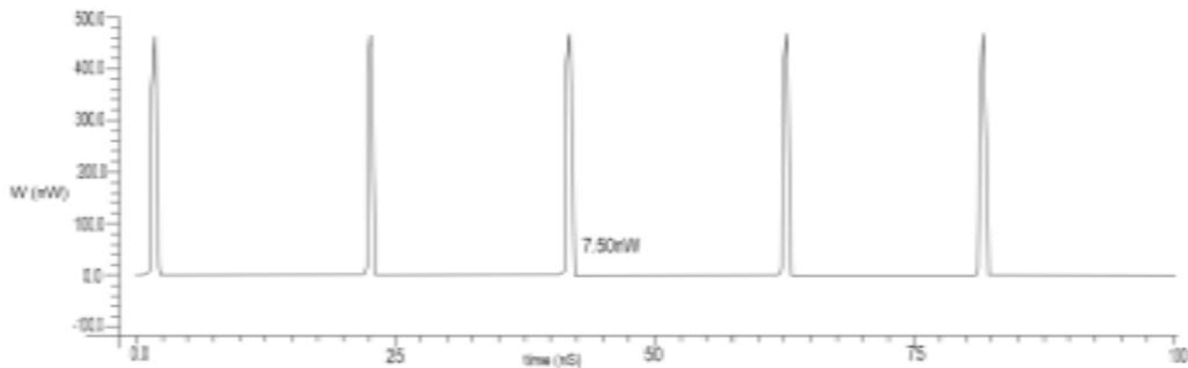

Fig 11: Static power dissipation by Hybrid technique on FinFET Based SRAM Cell

5. RESULTS:-

Improving the SRAM's leakage characteristics has been crucial to improving the cell's stability. Leakage current and power dissipation are reduced by 17.19% and 24.81%, respectively, using the AVL approach. The MTCMOS method lowers power dissipation and leakage current by 28.17% and 21.38%, respectively. By 25.59% and 31.29%, respectively, the suggested hybrid approach lowers leakage power and leakage current. The total leakage current and leakage power for several SRAM architectures are displayed in Table 2.

Table 2: Analysis of Total Leakage Current and Leakage Power for Different Leakage Reduction Methods

SRAM Topologies	Total Leakage Current	Leakage Power
6T FinFET	78.47×10-15A	10.922×10-9W
6T FinFET AVL	64.98×10-15 A	8.212×10-9 W
6T FinFET MTCMOS	61.69×10-15 A	7.843×10-9 W
6T FinFET HYBRID	58.39×10-15 A	7.504×10-9 W

6. CONCLUSION:-

In this paper**,** This work presents a unique leakage reduction method that outperforms FinFET-based 6T SRAM cells in terms of performance reduction and subthreshold current reduction. While traditional design and other design-based 6T SRAM cells with logic circuits are implemented in the noncritical route, the proposed SRAM cell has high threshold PMOS and high tox NMOS transistors in the critical path. Through simulation, a suggested design method based on 45-nm industrial FinFET technology is able to significantly reduce leakage power and leakage current by 31.29% and 25.59%, respectively, without causing an increase in path latency compared to FinFET based SRAM cells.

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