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IMPROVING POWER QUALITY IN ELECTRIC VEHICLES: INTELLIGENT METHODS EMPLOYING CASCADED MULTILEVEL INVERTERS

#1 Mr.AITHA RAJASHEKER Assistant Professor
#2 BETHI VAISHNAVI
#3 KODAMUNJA SAITEJA
#4 SYED ZUBAIR

Department of Electrical and Electronics Engineering,
SREE CHAITANYA INSTITUTE OF TECHNOLOGICAL SCIENCES, KARIMNAGAR, TS.

ABSTRACT: Power transmission is the method of transferring communication signals using power electronic circuits. This paper proposes a power transmission system based on cascaded three-phase multilevel inverters. By eliminating the need for a Controller Area Network bus to carry communication signals, the suggested solution lowers the infrastructure costs associated with the traditional electric vehicle (EV) communication system. The developed system is capable of balancing battery depletion and motor speed control for electric vehicles. This paper describes an Artificial Neural Network (ANN) controller constructed for a cascaded multilevel inverter. An electric vehicle (EV) system includes a DC link capacitor, which functions as a barrier between the rectifier and the converter. The EV system consists of a DC link capacitor at the rear and an AC/DC rectifier at the front. The charger's architecture allows for bidirectional power transfer, so the grid may manage voltage. The effectiveness of an ANN-based charger in regulating grid voltage to accommodate different charging and discharging modes for electric cars (EVs).

Index Terms—Battery state of charge, controller area network, frequency shift keying, motor speed control, pulse width modulation, three-phase DC-AC converter.

1.INTRODUCTION

Due to the issues faced by climate change, academics and professionals are actively investigating alternatives to fossil fuels with the goal of reducing carbon emissions. Presently, using electric vehicles in the automotive industry is a feasible way to cut pollution and conserve energy. Electric vehicles (EVs) emit fewer air pollutants, such as CO and NOx, than traditional internal combustion engine automobiles This trait is prominent in electric vehicles. Furthermore, replacing an electric vehicle's battery at night may prevent it from using electricity during peak hours, benefiting the grid in load balancing and lowering costs To enable communication between the transmission control unit (TCU) and various subsystems in an electric vehicle (EV), such as the motor control unit (MCU) and the battery management system (BMS) [an effective signal transfer technique must be designed. Manufacturers and researchers alike recognize the widespread usage of Controller Area Network (CAN) buses for data transfer in electric vehicles (EVs) due to their remarkable dependability and high communication baud rate.

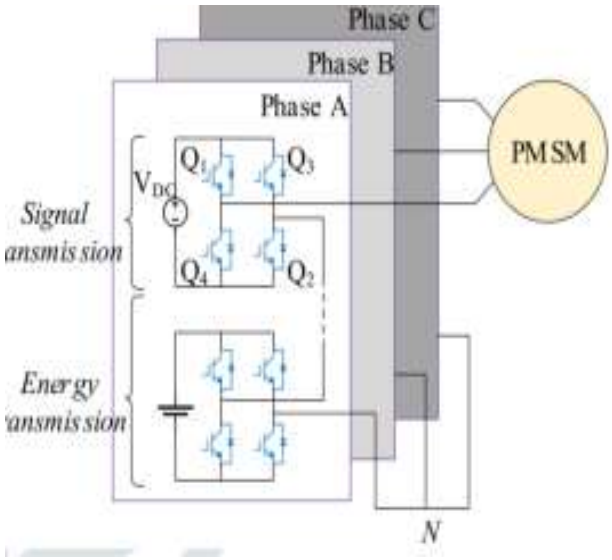


Fig. 1. The CBMLI of the proposed EV.

Figure 1 depicts the main configuration of an electric vehicle's powertrain. Certain typical EV power systems use a DC/DC converter to increase the battery voltage for a two-level inverter [8], [9]. The method's rapid voltage change rates (dV/dt) might result in considerable switching losses [8]. Furthermore, the use of large inductors in DC/DC boost converters increases the system's cost and reduces its power density [9]. Despite the fact that typical electric vehicles use the CAN bus for internal communication, the power transmission line and communication channel remain separate components, allowing for system optimization.

The three-phase multilevel inverter circuit built for electric vehicles (EVs) may transmit power and communication signals via the power & signal multiplex transmission (P&SMT) method suggested in this study. A DC/DC converter is unnecessary since the cascaded multilayer inverter can produce a voltage increase in the battery. The switching losses of the individual components of the multilayer inverter are much lower than those of a two-level inverter. The transmitted signals are modulated with frequency shift keying (FSK), and power conversion is accomplished using pulse width modulation (PWM) in the proposed system. In contrast to the CAN bus used by present EVs as a communication channel, the proposed approach transfers both power and signals via a single power line, potentially lowering the cost of the communication system.

2. PROPOSED POWER AND SIGNAL MULTIPLEX TRANSMISSION

A. System Structure

This article explains the fundamental principles of the P&SMT technique using a motor speed control signal and a communicated battery state of charge (SOC signal). Figure 2 depicts the suggested EV system architecture based on the P&SMT approach. Three-phase multilevel inverter circuits allow for communication between the motor and MCU, as well as between the battery and the BMS. Figure 3 shows the suggested architecture for a three-phase P&SMT system. The inverter architecture has four series-connected H-bridge cells per phase. Three of them are powered by batteries, with the remaining cell provided with a DC voltage supply to assist energy and signal transfer. The phase A and B branches carry the motor speed adjustment signal and the SOC signal, respectively. This model uses a permanent magnet synchronous motor (PMSM) to power the inverter design.

B. Signal Transmission

The proposed system modulates signals using the FSK approach, and Figure 4 depicts the signal transmission architecture. If the transmitted 4-bit signal SI is '1010', then two carriers with different frequencies denoted in SC can be used to modulate digital '1' and digital '0', respectively. Because the intended transmission of the signal over the H-bridge cell happens during each phase, signal modulation can be accomplished by rapidly switching the four switches within the cell. A switch becomes active in response to a digital "1" applied as a gate signal; the opposite effect occurs when a digital "0" is used to deactivate the switch. In Fig. 3, switches Q3 and Q4 turn on and off concurrently, whereas switches Q1 and Q2 do so simultaneously. Furthermore, to reduce the possibility of a brief circuit, switches Q1 and Q2 are configured in the opposite way as switches Q3 and Q4. The resultant current waveform has an overlaid look due to the series connection between the H-bridge cell used for signal transmission and the three cells used for energy transmission.

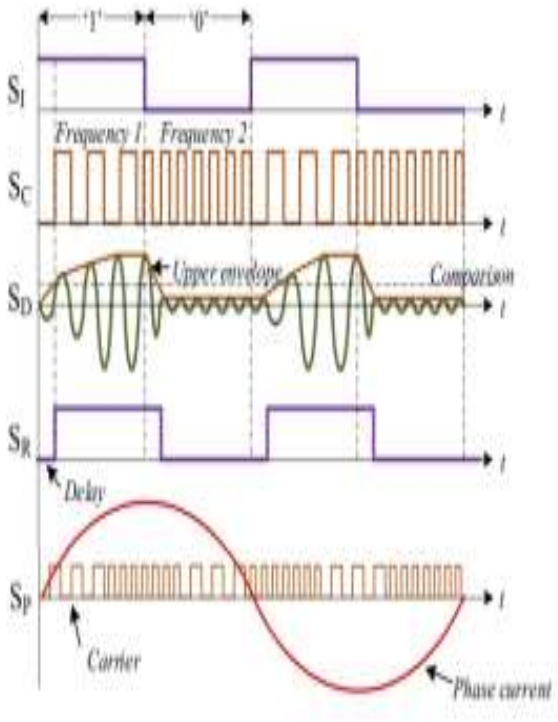


Figure 2 depicts the proposed system's signal transmission mechanism. The SI symbol represents the original 4-bit signal, "1010," but the SD symbol represents the recovered carrier for digital "1" after applying a band-pass filter. The SR symbol indicates the restored signal, whereas the SC symbol represents the output phase current waveform overlaid on the signal carrier. The transmitted signal is then retrieved from the receiver's output current waveform by applying a band-pass filter. The Fourier series expansion for a signal f(x) with period T and angular frequency $\omega=2\pi/T$ is as follows:

$$F(x)=\frac{1}{2}a_0+\sum_{n=1}^{\infty}\left(a_n\cos n\omega x+b_n\sin n\omega x\right)$$

where the coefficients and in this series are defined by

$$\begin{cases} a_0=\frac{2}{T}\int_{-T/2}^{T/2}f(x)dx \\ a_n=\frac{2}{T}\int_{-T/2}^{T/2}f(x)\cos n\omega x dx \\ b_n=\frac{2}{T}\int_{-T/2}^{T/2}f(x)\sin n\omega x dx \end{cases}$$

Similarly, digital "1" can be written as follows when the carrier wave is a square wave f(t) with period T.

$$f(t)=\begin{cases} 0 & -\frac{T}{2}\le t<0 \\ 1 & 0\le t\le\frac{T}{2} \end{cases}$$

The Fourier series expansion of f (t) is derived as

$$F(t)=\frac{1}{2}+\frac{2}{\pi}\sin x+\frac{2}{3\pi}\sin 3x+\frac{2}{5\pi}\sin 5x+\frac{2}{7\pi}\sin 7x+\ldots+\frac{2}{n\pi}\sin nx$$

In cases where n is an odd integer. The first-order harmonic can be used to restore communication signals because of its greater amplitude and the fact that the Fourier series expansion of f(t) only contains odd harmonic components. Figure 4 depicts an example of the demodulated carrier for the digital "1" as the SD curve, and an envelope detector can be used to obtain its upper envelope. When the upper envelope's amplitude exceeds the comparison value, the right comparison value can be used to restore it to digital "1". Failure to do so will result in its reversion to a digital "0." To retrieve the restored SR, the recovered digital signal is eventually sampled at the SI bit rate.

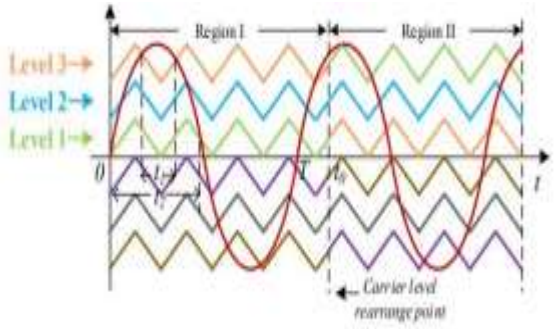


Fig. 3. Carrier level rearrangement in the PWM process.

Motor Speed Regulation and Battery Balanced Discharge The motor speed can be controlled by modifying the power frequency in the suggested system in response to the communicated signal. The relationship between the power frequency (f), pole-pair (p), and motor speed (n) of a PMSM is precisely specified as

$$n=\frac{60f}{p}$$

The constant 60 signifies 60 seconds each minute. A two-pole pair motor's speed should range

between 1200 and 1800 r/min if its power frequency varies between 40 and 60 Hz. The power frequency f is subsequently determined from the broadcast signal s.

$$f = 20 \times s + 40$$

When the transmitted signal contains the binary digits "0" and "1," the equivalent power frequencies are 40 and 60 Hz. The amplitude of the three-phase reference sinusoidal waves is represented by A, while the reference waves in phases A, B, and C are represented by Pa, Pb, and Pc, respectively. The phase A reference wave appears 2π/3 and 4π/3 radians before the phase B and phase C reference waves, respectively. In essence, modulated variable frequency sine waves are used to propel the motor and control its speed.

$$\begin{cases} P_a = A\sin(2\pi f) \\ P_b = A\sin\left(2\pi f - \frac{2}{3}\pi\right) \\ P_c = A\sin\left(2\pi f - \frac{4}{3}\pi\right) \end{cases}$$

The typical sinusoidal PWM approach is used to generate a switch's gating signal by comparing a triangular carrier to a reference wave. Because of the multiple sites where separate carriers and the reference wave intersect, each switch has a distinct duty cycle. Figure 5 shows that a switch modulated by a "Level 3" carrier has a lower duty cycle than one modulated by a "Level 1" carrier for a single period from 0 to T (t1 < t2).When powered by batteries, a switch with a lower duty cycle consumes less energy than one with a greater duty cycle. Furthermore, after some time of operation, the machine's battery will become imbalanced. Battery balance discharging can be accomplished by frequently rearranging carrier levels during the PWM process. To accomplish this goal, the battery state of charge (SOC) values at each periodic sample point are combined to form a data stream. This stream is then transmitted across a full-bridge cell driven by a DC voltage source using the FSK method. The phase current demodulates the signal, and the SOC values are fractionalized to several decimal places. To achieve battery balance discharge, for example, at time t0 in Figure 5, the PWM carrier levels are rearranged based on the communicated SOC values

3.ANN PERFORMANCE EVALUATION

ANN is a highly effective strategy for controlling the inherent complexity of nonlinear structures. To get optimal switching angles instantly, replace the look-up table with a properly built ANN [22]. Figure 5 shows a simple two-layer feed-forward network with concealed sigmoid neurons and linear output neurons that might be suitable for multidimensional mapping issues. An input layer is made up of N inputs, vector P, t1 sigmoid hidden neurons in the hidden layer, and t2 linear output neurons in the output layer. Figure 5 depicts the ANN's design, which has three layers: an input layer with two inputs, a concealed layer with two hidden neurons, and an output layer with two outputs. An ANN is used to create a Simulink model with a delayed feedback loop, as illustrated in Figure 6.

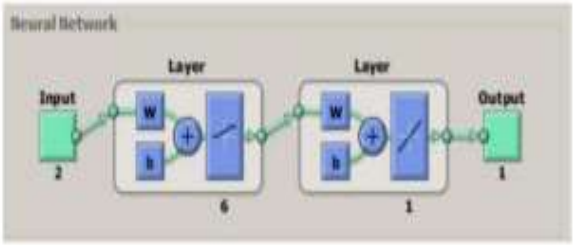


Figure 4. Simulink model for ANN-based neuron map chaotic system

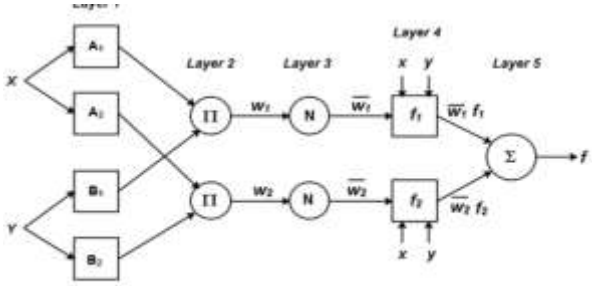


Figure 5. ANN controller block diagram

The network design of an ANN controller is governed by the number of neurons in each input, hidden, and output layers. The PWM generator uses the input from the initial output layer neuron to generate the proposed M-CHBMI switching signal. Wmij indicates the weight parameter for the connection between the ith and jth neurons in

the mth layer, whereas bmi specifies the bias parameter at the ith neuron in this layer. The transfer function of the network at the ith neuron in the mth layer is computed as follows:

$$n_i^m = \sum_{j=1}^{S^{m-1}} W_{ij}^m a_j^{m-1} + b_i^m$$

The output function of the MTH layer neuron can be characterized as

$$a_i^m = f^m(n_i^m)$$

The function of neuron activation is represented by f. In this architecture, the tangent hyperbolic function of the buried layer is defined as, while the output layer's activation function is set to unity.

$$f^m(n_i^m) = \frac{2}{1+e^{-2n_i^m}} - 1$$

4. SIMULATION RESULTS AND ANALYSIS

Waveforms of simulation parameters and output. Matlab/Simulink is used to create a simulation model based on the mechanics outlined. Table I shows the simulation model's parameter values. Each H-bridge cell used for power transmission is powered by a 48 V battery, whereas each H-bridge circuit uses a 30 V DC voltage source to enable signal transmission. As a result, the amplitude of the communicated signal is precisely at an appropriate level, preventing any major change to the output sinusoidal waveform while also allowing restoration. Furthermore, silicon-based IGBT devices are ideally suited for operation in this frequency range because they use carriers with frequency distributions ranging from 2 kHz to 10 kHz [20].

When a PMSM load is coupled to the output side of a three-phase inverter circuit, Figure 2 depicts the output voltage and current waveforms collected by a voltage and current sensor, respectively. The maximum phase voltage (348+30=174) is achieved by combining a DC voltage source and three batteries in each phase. The phase current waveform exhibits amplitude variations between 0.27 and 0.51 seconds. This is due to a frequency shift in the motor's output from 40 Hz to 60 Hz during these periods.

TABLE IPARAMETERS VALUE USED IN THE PROPOSED SYSTEM

Parameter name	Value
DC voltage source	30 V
Battery voltage	48 V
PWM carrier frequency	2 kHz
PWM referenced sine wave frequency	40 Hz, 60 Hz
Carrier frequency of motor speed adjustment signal	4 kHz for '1' and 8 kHz for '0'
Carrier frequency of SOC signal	6 kHz for '1' and 10 kHz for '0'

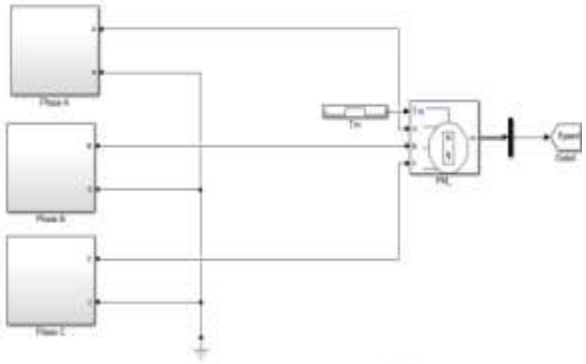


Fig 6. Simulation diagram of the proposed system.

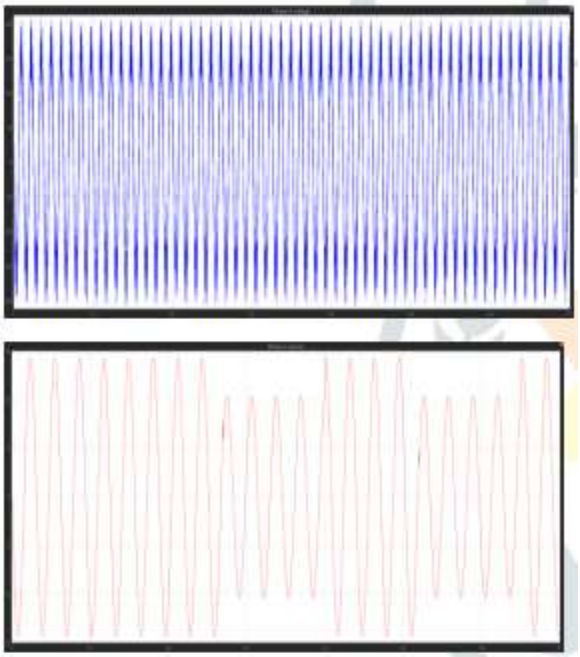


Figure 7(a) depicts the phase A output current and voltage waveforms.

Motor Speed Adjustment Signal Transmission

The initial 8-bit motor speed adjustment signal, set to 11110000 at a bit rate of 0.03 seconds, is transmitted at 100/3 bps. To distinguish between

two consecutive data strings, a cyclic redundancy code (CRC) of four bits is added to the end of each 8-bit data string. 111100000100 is the entire value of the 12-bit data frame, as the producing polynomial generated a 4-bit CRC code of 0100.

To detect whether the transmitted data frame is incorrect, the system may divide it modulo-2 using the divisor 11110 and check to see if the remainder is zero. If it is not zero, it indicates that there were no errors in the frame data during transmission; otherwise, an error occurred. Figure 3 illustrates both the original message data and the message data after the CRC code.

It is important to note that the transmission time for a frame with a CRC code is the same as that of a frame without one; hence, each bit of 12-bit data takes 0.02 seconds to travel. Digital "1" is broadcast by a 4 kHz square wave, while digital "0" is transmitted via an 8 kHz square wave after the whole data frame has been acquired. A band-pass filter separates the 4 kHz carrier from the phase current waveform after it passes through an H-bridge cell. Following that, the transmitted signal is recovered using the filtered carrier waveform SF shown in Figure 8 and the suitable threshold setting. Given that the band-pass filter's attenuation is constant at 6 dB at cut-off frequencies, the attenuation ratio x equals 0.5.

$$20\log x = -6$$

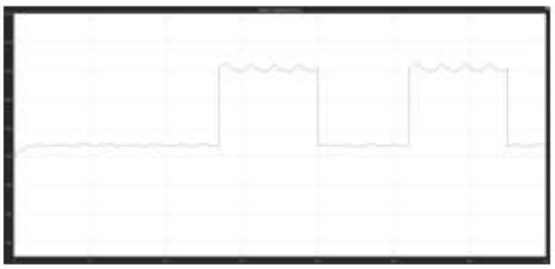
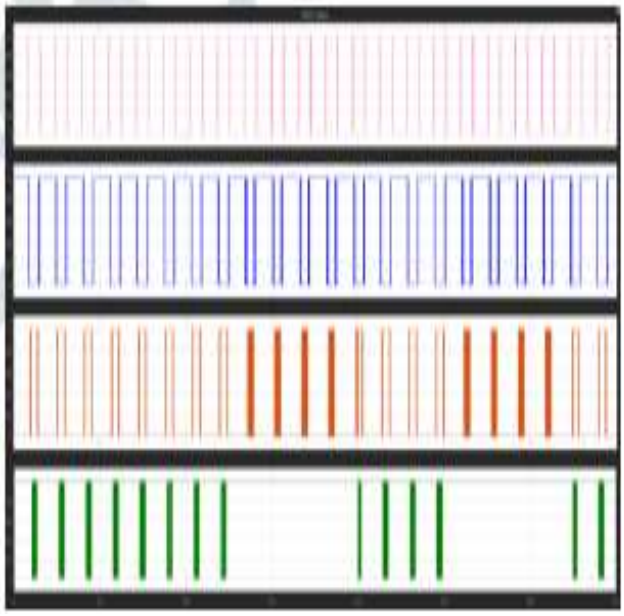


Fig. 8. The controlled motor speed with the transmitted 8-bit signal '11110000'.

In other words, the amplitude of the SF waveform is half in the passband frequencies (0.08) compared to the cutoff frequencies (0.04). As a result, the value "0.05" is used to distinguish the passband and cutoff frequency portions of the filtered wave. When comparing the SST of the recovered signal in Figure 4 to the SE waveform in Figure 3, there is a detectable delay in the SST, which is mostly due to the filtering procedure. Figure 4 depicts the restored signal SRE, which is produced by removing the 4-bit CRC coding from each 8-bit data frame.

During the initial time of 0.18 seconds (0.02×8+0.02 (one-bit delay)=0.18), the system "ignores" all data transferred prior to the 4-bit CRC code. Furthermore, the recovered data frame is processed at the same pace as the original signal (0.03 s per bit). SRE is defined as a delay of a whole signal period plus one sampling time, or 0.27 seconds (0.03×8+0.03 (one-bit delay)=0.27). At this point, the recovered 8-bit data frame becomes visible



The code string SCB consists of three SOC frames; the recovered SOC signal is designated as SRB; frame 01100100 in SBA1 represents the first battery's SOC; frame 00101000 represents the second battery's SOC; and frame 00100011 represents the third battery's SOC.

Finally, the waveform of the recovered signal SRE in Fig. 5, as shown in Fig. 6, determines the motor speed. Every time the signal changes from '0' to '1', the motor speed oscillates for about 0.01 seconds. As expected, because the power frequency is set to oscillate between 40 Hz and 60 Hz, the motor speed remains constant between 1200 rpm and 1800 rpm. The transmitted signal, which is in the form of energy, will disturb the phase current waveform and influence the stability of the motor speed. Furthermore, unlike the traditional double closed-loop control

strategy, open-loop regulation of the motor power frequency causes a more pronounced steady-state variation in the motor speed.

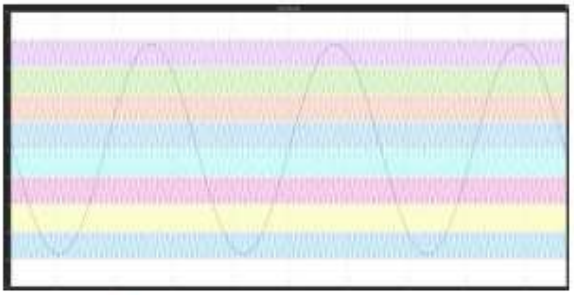


Fig. 10. The rearranged carriers and the reference sinusoidal wave used in the PWM process, where (a) is the original image, and (b) is the enlarged image at the carrier level rearrange point.

System Data Transmission Capability

The maximum data transmission rate for the proposed system can be calculated using the transmitted signal's error rate. A bit-by-bit comparison of the received and original data threads determines the sent signal's error rate. The incremental amplification of the motor speed control signal demonstrates the relationship between error rate and bit rate. As illustrated in this image, the error rate begins to rise once the signal rate exceeds 600 bits per second. The suggested system regulates the discharge process of the batteries based on their charge level, hence the precision of the communicated data is critical. Inaccurate data demodulation prevents the battery's SOC sequencing from producing the desired results. This system's data rate is relatively low when compared to traditional communication methods like optical fiber. Because the state of charge (SOC) of the batteries does not fluctuate considerably over short time periods, this system can withstand such a low data rate. Furthermore, delivering the motor speed control signal at a data rate of 600 bits/s is acceptable due to the temporal lag in motor speed normalization caused by frequency variations.

5.CONCLUSION

This study presents a P&SMT system based on a three-phase multilayer inverter to provide electric vehicles with battery balance discharge and motor speed control. The inverter architecture consists of four series-connected H-bridge cells per phase. Three of these are PWM-regulated and used for energy transmission, while the other four are FSK-regulated and used for communication signal transmission. However, unlike the ANN method, the switching angles of the ANN technique result in less total harmonic distortion (THD) in the output voltage waveform of the improved CHBMLI. However, because to the ANN method's simple and effective switching angles, the upgraded CHB-MLI output voltage and current waveform has a lower THD content. The suggested P&SMT method is tested by sending the motor speed adjustment signal and the battery SOC signal through phase-A and phase-B currents, respectively, in a Matlab/Simulink simulation model.

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