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DESIGN AND IMPLEMENTATION OF ACCURATE HYBRID KS WITH CS ADDER FOR HIGH SPEED OPERATIONS

[1]S.VASANTH KUMAR REDDY, [2]R.RAMA MOHAN, [3]Dr.P.SREENIVASULU
[4]A.SANDEEP KUMAR REDDY, ,
[1,4]M.Tech Scholar, Dept of ECE, Audisankara College of Engineering and Technology, Gudur, Andhra Pradesh
[2]Associate Professor Dept of ECE, Audisankara College of Engineering and Technology, Gudur, Andhra Pradesh
[3]Professor Dept of ECE, Audisankara College of Engineering and Technology, Gudur, Andhra Pradesh

ABSTRACT: In complex data processing, the basic elements which are known as adders are used for efficient VLSI design. For high speed design processor the CS (Carry Select) adder circuit is used. In CMOS technology, by preserving the circuit speed there is a scope for decreasing the design area and power. The architecture of CS adder is such that it is of high speed, efficient area, and less power dissipation. In a number of computer systems the Carry Select Adder (CSA) is used by producing numerous carry bits to reduce the impact of carry propagation delay and for the required output picking a carry. In integrated circuits one of the most important design objectives is known as power dissipation, after area & speed. In such circuits the most widely used components are known as adders, for researchers the efficient adder design is much concern. In this work, for high speed operations the CS adder with accurate hybrid KS (Kogge Stone) implementation and design was presented. To obtain higher speed hybrid CSA design was presented in this work, which utilizes both Carry Look ahead Adder (CLA) and Kogge Stone adders advantages. A particular type of adder is known as Kogge stone adder and hence, due to faster carry generation one of the high speed addition method was regarded widely. In the modified adders initial stage, the look ahead adder was employed to boost its speed, if the number of bits are less then its computation performance is better.

KEYWORDS: Carry Select (CS) adder, Adder, Kogge Stone, Carry Look ahead Adder (CLSA).

I. INTRODUCTION

In today's technological environment, the requirement in the area of portable gadgetsand consumer electronic for energy efficient computations, quick and inexpensive is becoming more and more common. To create high speed computation techniques is the goal with area overhead and little power. In digital processing systems and computers, one of the most basic operations is addition, and it often calls for adders, or several arithmetic units [1]. In arithmetic logic unit (ALU), a prominent arithmetic operation is known as binary addition in modern microprocessor. Subtraction, 8 division, magnitude comparison, multiplication, and in their intermediate stages many more arithmetic operations need addition. To maintain processor performance the digital blocks computing speed was ensured that is an obligatory requirement. Since, in several binary arithmetic operations a pivotal part was played by adder, in improving the overall ALU performance the adder circuit's energy-efficiency design will assist with high speed. The basic digital systems element was considered as adder, based on

adders there are most of the arithmetic operations [2].
The performance of digital systems and a fundamental mathematical operation can both be significantly impacted by addition. Most electrical applications make use of arithmetic processors, or adders. Uses for these include multipliers and digital signal processors for running algorithms like FFT, FIR, and IIR [3]. The presence of adders is essential and well known in contexts involving the concept of multiplication. It is well knowledge that microprocessors can execute millions of instructions every second. As a result, the need for quick calculations is the primary limitation placed on multiplier design [4]. The portability of the devices necessitates a high degree of miniaturization and a low rate of power consumption. More battery life is needed for devices like mobile phones, laptops, etc. By optimizing the adders design the systems total performance can be sorted greatly in aspect of their energy consumption, delay, and size [5].

In system, a huge advancement can be provided by enhancing adders. So far in findings, a large adder's architecture variety is accessible. A high speed adder is known as CS because of its minimized power consumption and small size [6]. As the simplest and also the most basic binary adder the RCA (Ripple Carry Adder) is considered. In a ripple carry adder found the main problem to transport a carry along this adder is addition speed dependency of these adders with the need of time. In time-critical applications mostly employed the carry look-ahead adders, which requires large combinational logic at the cost of more area. Among the speed characteristics and size requirement, a better tradeoff was shown by the carry select adder [7].

Within electronic devices, the modern integrated circuits (IC) with limited power dissipation it needs high-speed operation [8]. Therefore, in present-day ICs the crucial parameters are considered as the power and speed. However, the necessary speed was maintained because of the modern portable devices high integration density requirement and for circuit designers, having the acceptable power appear to be a challenging task. Due to this, to cope up with the ever-changing requirement the new circuit evolution became inevitable [9].

The key performance indicators for high-performing digital electronic circuits are occupied by the circuit, power dissipation, and speed. With smaller dimensions and fast speed the portable devices are expected to have reasonable power usage apart from being smaller [10]. As a result, between the digital circuits performance parameters the circuit designers face some tradeoffs, which means that the other might get affected in order to improve one parameter. Along with high-performance, the portable devices main requirement is high computational capacity. Therefore, a small circuit developing might become a difficult task to a circuit designer with fast operation and low power dissipation [11].

Researchers are emphasized highly on their logic level designs and on CLA algorithms, whereas to improve transistor level design a very few attempts have been taken [12]. Simultaneously, by generating various carries parallel avoids the delay due to carry propagation in carry select adder and to create the corresponding output the apt carry value must choose [13]. However, utilized more than one basic adders pairs which are founded by the CSLA as it is not compact, the value of input carry Cin=1 and Cin=0 to output the summation as well as

intermediate carry. In terms of delay a better performance was shown by implementing CSLA with PPA (Parallel Prefix Adder). Therefore, several adder logics were incorporated within the hybrid CSA architecture that can improve the CSLAs design efficiency rather than realizing pure CSAs. Hence in this work, for high speed operations the CS adder with accurate hybrid KS implementation and design was presented.

As follows, the rest of the work was organized that is: The literature survey was described in section II. For high speed operations the CS adder with accurate hybrid KS implementation and design was presented in section III. The result analysis was evaluated in section IV. Finally, in section V the work is concluded.

II. LITERATURE SURVEY

M. I. Kollannur, M. C. Joy, A. Jimmy, and T. C. Thomas, et. al., [14] for High Speed Operations a Carry Bypass Adder Architecture and Modified 16 bit Carry Select was described. In this work, in terms of their delay, the existed different 16 bit adders are compared. Using logical effort the logical gates delay of mathematical modeling has been done in 180nm. While simulating in Modelsim, the different adders delay was obtained using this delay. Using Modelsim the adder's functional verification have also been done. For each adder the Xilinx ISE was used to find out the path delay. In the light of this analysis, to achieve less propagation delay proposed a carry select adder and new carry bypass adder. In combinational path delay, decrease of 16.5% and 45.42% and respectively, in logical effort delay, 29.5% and 20.4% was shown by the proposed carry bypass adder and carry select adder.

N. Takagi and N. Kito et. al., [15] with easy Testability, the Concurrent Error Detectable carry Select Adder was described. Based on multi-block carry select adder, an adder was proposed. Compared with the predicted sum parity, by a fault modeled any adder's erroneous output which is caused can be detected as a single stuck-at fault with the sum parity, i.e., the value of the XORed sum bits, and the duplicated carry outputs are also compared. With only 10 input patterns, the adder is also testable under single stuck-at fault model. Before the occurrence of a second fault, this property eases fault detection. For realizing reliable systems, both the concurrent error detectability to easy testability and detect erroneous results are important to find a fault during operation. The proposed adder's both easy testability and concurrent error detectability has been proven. Designed a 32-bit adder.

A. Dube, S. Sreshta and D. Singh et. al., [16] with carry select adder, Dual-pair-single-rail-checkers implementation and design was presented. To provide more area efficient adder and efficient fault analysis a carry select adder and a multi-bit-self-checking sum were designed. Using Cadence® Virtuoso platform the analyses and simulation are done with gpdk180nm technology library. Respectively, the proposed Carry Checker 2 has a delay of 100 ns and a power of 454 μW. With a Carry Select Adder, when it was implemented then they both are less than the conventional checker. At the output, this makes the adder circuit inherent and mandatory part in avoiding faults. As that of the modified and conventional circuits, the delay is almost equal.

Rashmi S.B and V. Oli et. al.,[17] using 4T XNOR gate a 32 bit power efficient carry select adder was described. For 32-, 8-,16-

bit a hybrid CMOS Full Adder circuit is used to design the CS circuit and delay, area and power are the parameters compared with the regular CS. Here, in the regular CS the excess logic operations are eradicated and before the final sum calculation a new logic operation was proposed that was formulated for the modified CS. Respectively, by the modified Full adder and XNOR the power consumed is 1.273mW and 0.5595mW. Compared with the conventional CS, the modified CS is more efficient in terms of delay, area and power that was shown by the results. For high bit word size this work need to be extended further and to reduce the circuit delay and area power, applied different optimization techniques.

Poovanan E, Lavanya K, Sasikala U.T, Ramkumar Prabhu M, and Rajalingam A, et. al., [18] Low Power High Speed Carry Select Adders performance analysis was presented. Using gate-level modification, developed the modified CSLA to reduce significantly the power and delay of CSLA. Developed a 128-, 64-, 32-, 16-, and 8-bit square root Carry Select Adder (CSLA) architecture based on this modification and with regular carry select adder architecture it was compared. Compared with modified and regular square root CSLA, for higher adder the delay and power has reduced by the proposed design. To simple gate level modification it is proposed, by 19.4% the power will be reduced significantly for 256-bit addition. Specially, this paper concentrates on CSLA's area constraints and speed.

M. Vijayaraj, E. John Alex, et. al., [19] for biomedical process a BEC Modified Carry Select Adder's energy efficiency based PTMAC architecture was presented. Binary to Excess-1 converter is used to reduce power which is the main of this paper, to reduce the Carry Select Adder's area and power to a tolerant level a proficient and uncomplicated gate-level adaption was used. Compared with the Regular Square Root CSLA, Conventional CSLA and Modified Carry Select Adder of BEC, the proposed design proves to be better based on the analysis. Moreover, For low power biomedical instrumentation the Accumulator Circuit architecture and Programmable Truncated Multiplexer are used, with a need they are designed for reticent digital signal processing like EEG filtering, detection of ECG fall and others by using the BEC modified CSLA. In a DSP architecture, efficiently proven that the BEC modified CSLA through its implementation with the combined fault tolerant beniefit.

Rohit Khare, Sandip nemade et. al., [20] for High-Speed Applications an efficient 64-bit Carry Select Adder Design of an FPGA based Area-Delay was presented. With low power combinational design, a Carry-Select-Adder (CSA) design is presented. For its power and functional performance the design is simulated and synthesized on Field Programmable Gate Array cased VLSI hardware. With some existing work, the power analysis and comparative speed of the proposed work was presented in the present study. On the basis of the proposed work, concluded the FPGA based low power analysis. Using Xilinx Tool, performed the present work.

Vijjapu Anuragh & Pudi Viswa Santhi et. al., [21] High Speed Hybrid Sqrt Carry Select Adder Design was described. Different Fast Adders performance analysis was presented in this paper. On the basis of three performance parameters, the comparison is done i.e. Power consumption, Area, and Speed. In different stages designed a presented modified carry select

adder. From modified carry select adders obtained the results which are better in power consumption and area in comparison with Regular CBL-CSA, CSA, BEC-CSA. Using Xilinx 14.7, at 90nm process technology targeting it has been synthesized the design.

P. Balasubramanian, V. Kokilavani, and K. Preethi, et. al., [22] High-Speed Hybrid Carry Select Adder's FPGA-Based Synthesis was presented. In Verilog HDL, implemented Seven different carry select adders and analyzed their performances under two scenarios, multi-operand addition and dual-operand addition, where 64and 32 - bits are the sizes of individual operands. The proposed section carry and carry select based carry look ahead configuration was comprised by the hybrid carry select adder which is the fastest in the case of dual-operand additions. Similar optimized performance will be produced by the hybrid carry select adder that containing section-carry based carry look ahead or conventional carry look head and carry select structures with respect to multi-operand additions.

S.Allwin Devaraj, R. Helen Vedanayagi Anita, S.Abirami et. al., [23] with reduced power and area, the carry select adders design was described. By pass transistor logic (PTL) technique the proposed CSLA is being designed for further power and area reduction. For each logical circuit the number of transistors used is reduced by using pass transistor logic so that for the carry select adder the power consumption and area has been reduced. Using Tanner EDA tool the simulation is carried out.

Yogita Hiremath et. al., [24] using 180nm CMOS process technology, a novel 8-nit Carry select adder was presented. An efficient high-speed 8-bit carry select adder was presented in this paper. Using 180nm CMOS process technology the adder is implemented and designed. A good compromise was provided by the proposed adder between the performance and cost in carry propagation adder design. Compared to the ripple carry adder, the computational time decreases and thus the speed increases. An array of 2:1 multiplexers and 4-bit ripple carry adders are consisted in the carry select adder. Through the multiplexer the carry is selected. In terms of area the design layout is efficiently optimized using micron rules of CMOS 180nm technology. In terms of different parameters performance analyzed the blocks and adders performance. The transistor count, power consumption and propagation delay of the adder was found according to the estimations done that to be 13.77µW, 246 and 340ps.

Gagandeep Singh and Chakshu Goel et. al., [25] using 3-T XOR Gate an Efficient Carry Select Adder and Low Power Design was described. A carry select adder (CSLA) at low cost is the most suitable to perform fast addition operation among the conventional adders structures. In this paper, in designing higher bit adders a 3-T XOR gates is used, it is an essential blocks to design an 8-bit CSLA as XOR gates. As compared to modified CSLA and regular CLSA, there has a lesser power consumption and has reduced transistor count as well as power-delay product (PDP) to the proposed CSLA.

III. DESIGN AND IMPLEMENTATION OF ACCURATE HYBRID KS WITH CS ADDER

In this section, design and implementation of accurate hybrid KS with CS adder for high speed operations is presented.

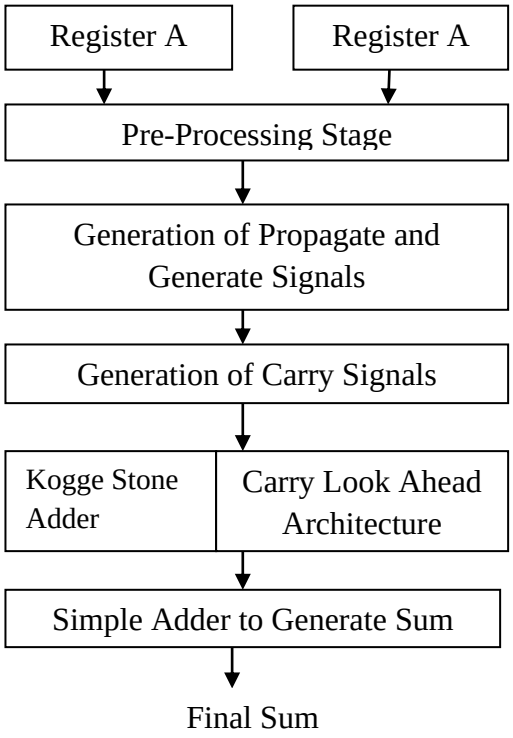

Figure 1: Block Diagram of design and implementation of accurate hybrid KS with CS adder

The figure 1 shows the block diagram of accurate hybrid KS with CS adder for high speed operations. In most of the arithmetic units, employed the utmost common structure of adder that was considered as the CS adder it decreases the propagation delay. By using redundancy two numbers are added, behind the carry select adder this is the basic logic to speed addition. That is, performed two additions process for any number of sum bits, one taking c-in as '0'and the other c-in as '1'. With B=B(N-1)……..B(0) and A=A(n-1)……..A(0) the addition of two n-bit numbers are considered. The most complex logic is required with the (n-1), from the 0^{th} position of least significant the adder delay increases to upward at the bit level. The addition problem was broken by a carry select adder in to smaller groups.

The computation of the generate and propagate for carry bit of each adder is carried out in this stage. Let A and B as input, the carry generate and propagate terms are expressed by the equation

$$P_n = A_{n-1} \dots\dots A(0) xor\ B_{n-1} \dots\dots B(0) \quad (1)$$

$$G_n = A_{n-1} \dots\dots A(0) and\ B_{n-1} \dots\dots B(0) \quad (2)$$

The computation of carry output corresponding to each bit in this stage is carried out in this stage. The above execution is performed simultaneously. Later they are divided into little slices. Each carry operator consists of two numbers of AND and one number of OR gate. Propagate and generate signals are utilized as halfway signals which are expressed by the following equations

$$P(n:k) = P(n:m) and\ P(m-1:k) \quad (3)$$

$$G(n:k) = G(n:m) or\ (G(m-1:k) and P(n:m)) \quad (4)$$

A type of logic adder is known as CS adder that computes the sum of 2 n-bit adders (n+1)-bit. In long chains the addition process is broken down into small groups in CSA. Mainly divided a n-bit CSA is into (n/2)-bit section. The carry bit can have two distinct states in the binary carry generation: logic 1 and logic 0. Therefore, Cn/2 bit carry will also have those 2 distinct states

$$C_{n/2} = 1 or\ C_{n/2} = 0 \quad (5)$$

The problem of n-bit can split into two (n/2)-bit-selections, to the higher order group it gives special attention that adds the word segments B(n-1)…….....B(n/2) and A(n-1)……A(n/2). By the sum of lower order word segments A(n/2-1)…….....A(0) and B(n/2-1)…..…B(0) produces the carry delay will then center around the carry-out bit C(n/2). We now that, for the carry bit there are only two possibilities, c(n/2)=1 or c(n/2)=0. For the upper words the two separate adders (CLA and KS) are provided

by a carry-select adder, one for each possibility.

A hybrid carry select adder is a proposed adder, more than one adder architecture is used to attain higher speed. To take advantage of to adders the Hybrid adder is designed namely CLA and Kogge stone adder. To the category of fastest adder the Kogge stone adder is belonged that was used in KS adder because employed the carry generation method much faster. The fastest addition logic was provided, to boost its speed the CLAs are employed.

As a high-speed adder the Ks adder is commonly treated, and to the parallel prefix adders group it belongs. For performing computations and higher complex arithmetic operations the KS adders are suitable. Carry is generated and calculated in the Kogge stone adder simultaneously at the increased possibility area at the rapid pace. A conventional apt architecture was possessed by a KS adder so, to the existing technology and electronic circuit it is adaptive. Moreover, there has least fan-out to the KSA which has the main advantage. Thereby, in computation it is faster but requires more size. Utilization of area is high for KS adder, even though to a great extend the delay will be reduced.

The addition operation was speeded up by the Carry look-ahead adder based on the input signals, in this scheme for the next stages carry is calculated in advance. In RCA, to eliminate the ripple effect a way was offered by the CLA. In the proposed adder there has an essential role in CLA; in the proposed hybrid adder, employed the CLA to make it speed optimized. To perform the addition process speeded up the operation by the carry look-ahead algorithm. CLAs are those adders, depending on the values of input the carry is calculated earlier for all stages. Carry generate and propagate are the two separate elements on which the CLA algorithm relies.

Provided the proposed adder with inputs Register A, Register B. The two input registers are A and B which are to be added. By the combination of CLA and Kogge stone the addition was performed in each stage to provide two possible values for carry and a simple adder is used to calculate a corresponding output. Simultaneously, in the two stages the operation of addition takes place. To the selection unit the obtained sum and carry was fed, an appropriate carry will be selected and outputs the count and sum.

IV. RESULT ANALYSIS

In this section, design and implementation of accurate hybrid KS with CS adder for high speed operations is presented. The presented adder performance is measured in terms of delay, area and PDP (Power Delay Product).

Power Delay Product (PDP): PDP is simply the delay and power consumption product. Therefore, by the circuits propagation delay the average power is multiplied to obtain PDP.

The Figure 2 shows delay performance comparison.

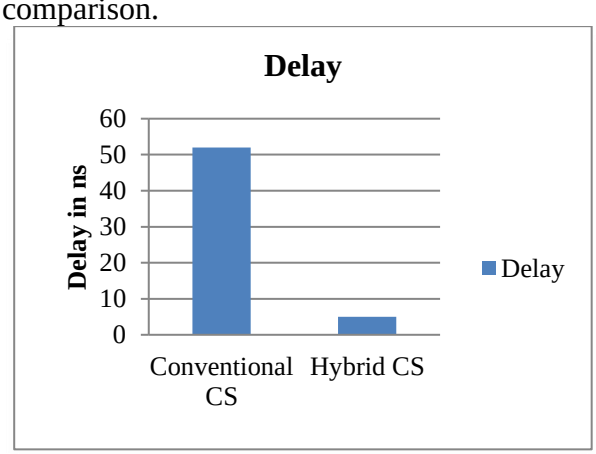

Fig. 2: Delay Performance Comparison

In Fig. 2, the x-axis represented Conventional Carry select adder and Hybrid CS adder whereas y-axis indicates delay performance in terms of nano seconds (ns). Presented Hybrid CS has very less delay compared to conventional CS adder. The Figure 3 shows power comparison.

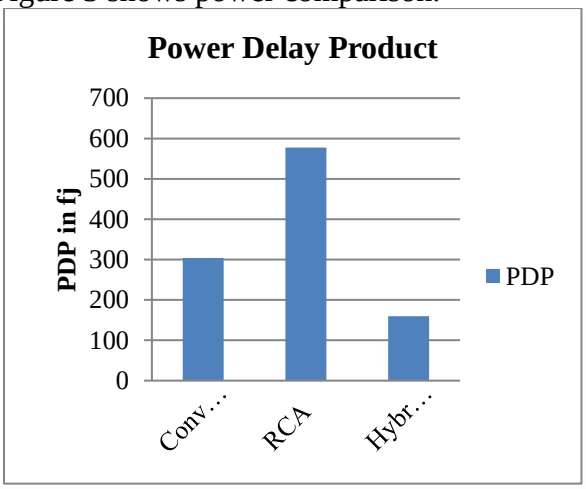

Fig. 3: PDP Comparison

The hybrid CS adder has very less PDP than conventional CS adder and RCA. The Fig. 4 shows area comparison.

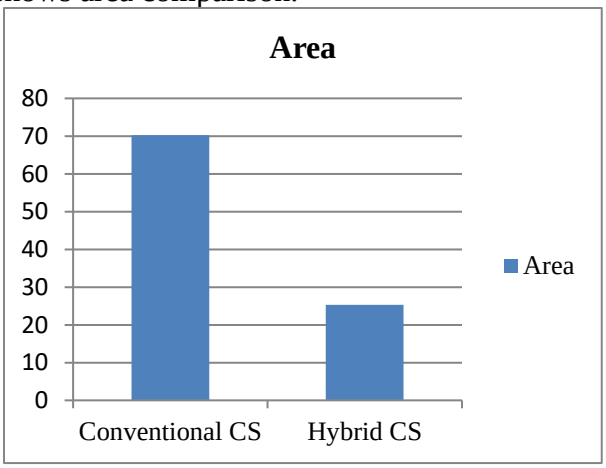

Fig. 4: Area Comparison

In Fig. 4, the area performance is measured in terms of μm^2. Compared to conventional CS, presented adder has very less area. The Figure 5 shows speed performance.

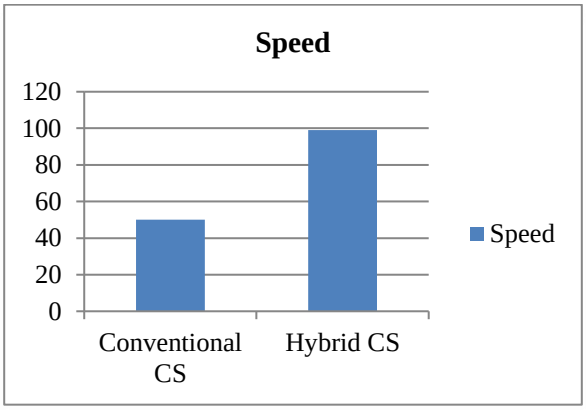

Fig. 5: Speed Performance comparison

The speed of hybrid CS adder is improved significantly compared to conventional CS. The Hybrid CS adder has very less delay, PDP, area and very high speed.

V. CONCLUSLION

In this work, design and implementation of accurate hybrid KS with CS adder for high speed operations is presented. Compared to other existing structures of CS adder, to a great extent the power consumption and speed was improved by the CS Adder that is the fast adders combination like CLA and Kogge stone adder. A particular type of adder is known as Kogge stone and due to its faster carry generation, it is regarded widely as one of the high speed addition method. To boost its speed, employed a look ahead adders. The computational time reduces efficiently by the carry select adder and thus the speed increases. In terms of Area, delay and power delay product (PDP), analyzed the design performance. In terms of power delay product, delay, and area, the best performance was showed by this CSA adder. Hence, in high-performance ALU design this work can be highly useful in modern systems.

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