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Parameter Optimization Of Analog Circuit Implementation Using Neural Network Models

By

Varghese M P
Research Scholar, Department of Electronics and Communication Engineering, Vinayaka Mission's Research Foundation Deemed to be University, Salem, India

T. Muthumanickam
Professor & Head, Department of Electronics and Communication Engineering, Vinayaka Mission's Kirupananda Variyar Engineering College, Vinayaka Mission's Research Foundation Deemed to be University, Salem, India

Abstract

Designing analog integrated circuits is frequently thought of as a time-consuming task due to the fact that transistor and passive component dimensions have a significant impact on analog performance. Several automation techniques have been used over the past ten years to conduct extensive research on the analog circuit front-end design cycle. Machine learning is now a desirable and practical solution for everyone due to significant advancements in high-performance computing technology. The goals of this survey are to provide a comprehensive overview of the most advanced machine learning techniques currently used at the analog circuit scale and analyze how well they perform in terms of achieving the desired goals and identify the most critical areas for future research. Find nodes in a neural network that maximize the objective function and minimize the objective function. To demonstrate the effectiveness of the optimization strategy using outcomes from integrated circuit applications of ANNs, we classify digital data that has been simulated in PSpice.

Introduction

Electronic design automation (EDA), a crucial area of electronics engineering, is still very active and uses the most recent technologies and algorithms. Integral circuits (ICs) have grown in size significantly over the past few years as a result of advancements in semiconductor technology, posing challenges to the circuit design process's scalability and reliability. Because of this, extremely large, low-latency spaces require searching methods that are more efficient and effective. Problems involving classification, detection, and design space exploration can be resolved using ML techniques, including deep learning and conventional learning algorithms. Rather than repeatedly running complex analyses, ML algorithms place a greater emphasis on gathering patterns or features that are common or that can be applied in related or comparable contexts. The application of machine learning strategies that expedites an EDA problem solution is a promising area. The research that has been gathered can be divided into four categories: black-box optimization, automated design, traditional decision-making methods, and performance prediction [1]. Using traditional methods for decision-making, the ML process in EDA begins. Instead of using empirical selection, ML models are trained to select from a set of available toolchains, algorithms, or hyperparameters. Using ML to prognosticate performance, estimate new designs without having to go through the time-consuming conflation process. Using a database of enforced designs, a model is trained to forecast the quality of new designs [2]. Design Space Exploration (DSE) has been further automated by EDA technology using a black-box optimization approach, where prophetic ML

models and slice strategies based on ML proposition drive the entire DSE process. Recent advancements in deep learning (DL), particularly reinforced learning have sparked a great deal of investigation into the complete automation of some complex design tasks in genuinely large design spaces[3]. These studies indicate a bright future for automated design that is supported by artificial intelligence (AI), where programs and predictors are learned, used, and adjusted online.

Creating circuit layouts, performing manual calculations, running circuit simulations, running parasitic simulations, and replicating circuit inputs and outputs are all steps in the design of complementary metal-oxide semiconductor (CMOS) circuits [4]. Instead, they might alter as new and improved circuits are created and applied. This is the end result of efforts to lower costs and boost manufacturing performance for the design. The type of chip and the needs of the end user may also be relevant [5]. Usually, significant design changes cannot be made once the chip is in production. As a result, CMOS has emerged as the technology most frequently utilized in VLSI crisps [6,7],8. A VLSI design with low power consumption is the end result. Although hardware is anticipated to realize benefits of ANNs, the majority of neural network advancements come from theoretical research or computer simulations. To illustrate how the general approach is applied, a case study of digital pattern classification using multilayer ANNs is used [9]. Electronic simulations of PSpice-built integrated circuits indicate the viability of this optimization method. Making circuits for multilayer ANN training models using operational amplifiers through CMOS transistors as the fundamental building blocks. Verification of integrated circuits (ANN hardware) created using Pspice results from electronic simulation [10]. A multilayer ANN (automatic learning method) based on gradient descent that simulates the tuning of the bias and weight parameters to achieve convergence. A multi-layer ANN hardware case study that categorizes digital patterns can be used to simulate data transmission to see if it is functioning properly.

The fact that almost all optimization issues can be numerically resolved through an iterative process is well known. Since the learning rate can be arbitrary high without endangering the stability of the system, continuous systems have stronger convergence properties. Contrarily, discrete-time systems only need the control parameters to be constant for a short while. Otherwise, the system might become unsteady. Systems of dynamical equations with fundamental differential equations are more resistant to changes in some parameters [11,12].

Analysis And Development:

Effective placement assignments may lead to increased conductivity, chip area utilization, and clock performance. Placement assignments indicate that routing is a critical phase in the VLSI physical design cycle. The wires connecting the components of the chip are assigned through routing [13]. Additionally, routing must adhere to design standards while also fulfilling specifications for timing performance and overall wire length. Routing and placement go hand in hand. As a result, it is crucial to take routing efficiency into account at the placement stage. To enhance the performance of physical designs, several ML-based routable approaches have been presented. Fabrication is a labour- and resource-intensive process that calls for numerous intricate steps [14]. Mask synthesis is one of the most important fabrication processes, and to lower the possibility of fabrication errors, lithography simulation is used. Mask optimization and lithography simulation remain challenging problems. For the synthesis of masks and simulation of lithography, several methods based on ML have recently been applied [15]. The design should be checked to make sure it is accurate before fabrication. Every phase of the EDA cycle is typically followed by verification. One of the key issues is

verification set design. The traditional automatic or random test set generation methods are not ideal, so ML techniques have been used in a number of studies.

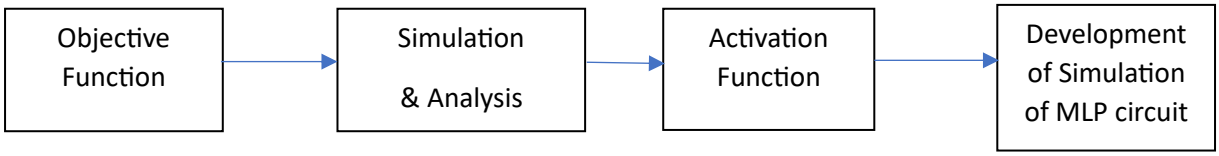

Fig. 1. *Block diagram of the proposed circuit design*

Figure 1 displays a block diagram of the suggested method for designing circuits. The numerical analysis and simulation steps that went into optimizing the objective function (determining synaptic weights and ANN biases) are represented by these terms in Block 2. Block 3 concentrates on the circuit level development of fundamental neurons (perceptron). The final step to achieving the behaviour of the NN suggested in the study is complete MLP circuit design and simulation demonstration in Block 4.

A multivariate polynomial regression model is used to forecast circuit performance in a new context after first estimating the performance trade-offs of the optimization. The NN is then given the results. The NN learns how to predict device size based on the improved performance by using the updated samples as training data. Data processing comes first. Both training dataset and a test dataset are required to enable ML for HLS estimation [16,17,18]. The second step is to train the estimation model. A regression model is trained to predict the post-implementation resource utilization and the heartbeat period after the dataset is created. It is customary to use the relative absolute error (RAE) and relative root mean square error (RMSE) to denote estimation error. The lower the number, the better for both measures. The resulting samples are randomly divided into three sub-data sets at the beginning of the training process. This dataset is used in training (70 percent of the training set), Validation set (15 percent). This dataset is used to validate and generalize assumptions [19,20]. It also influences how the training process is completed. Test Set (15 percent): After the training phase, this data set is used for another evaluation test. In order to simulate various operating conditions for the circuit, you can alter the stimuli and device parameters. It is possible to simulate the entire circuit to assess the performance of the entire network after modelling. In order to achieve this, the synaptic and activating mechanisms are coupled to create a bipolar input vector in the manner.

Result

The hardware density of the architecturally designed components is directly correlated with power consumption. In our approach, only operational amplifiers and resistors contribute to the power consumption. The transistor cell controls power consumption, and signal propagation delay's impact cannot be disregarded. Last but not least, power usage for FPGA implementations [21] was influenced by the number of programmable logic gates present throughout the system, and both static and dynamic power must be taken into consideration. Few architectures make use of all of an FPGA's hardware resources, so some devices continue to draw power even when no longer in use. The calculations are carried out by the neurons. It uses roughly the same amount of energy as was stated. While the simulations in our work and were carried out in Pspice and Matlab, respectively, they cannot be directly compared. Both cases used different application methods and techniques[22]. But it makes sense to assume that as technologies like memristors advance, energy consumption will decline. Although has a high

energy consumption, numerous publications, including claim that efforts are being made to reduce it.

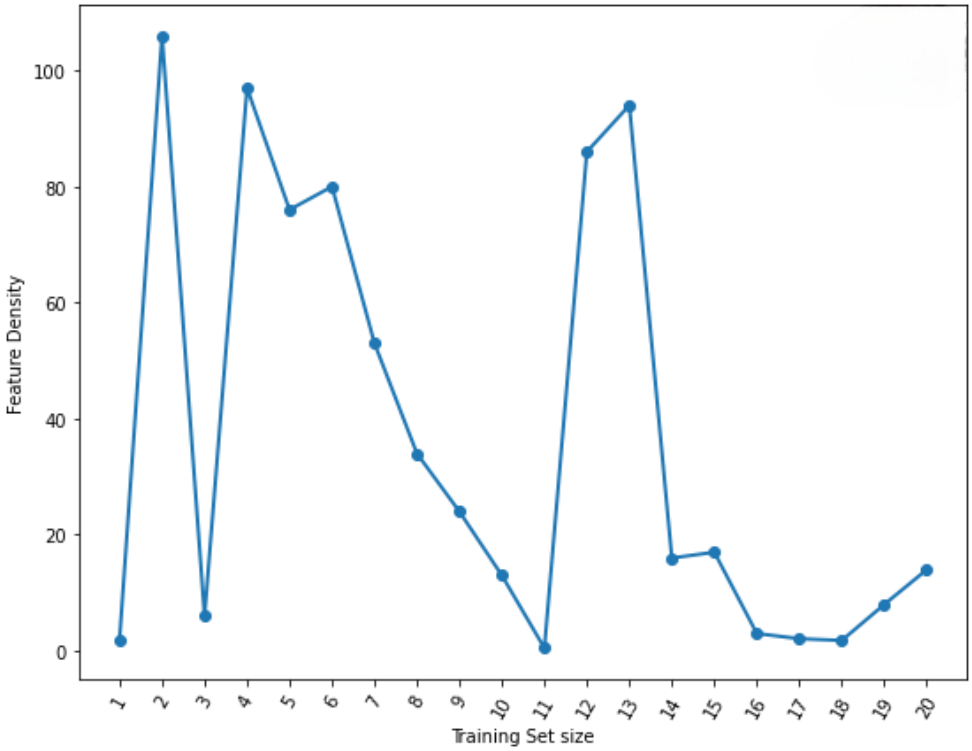

Fig. 2 *Feature Density vs Training set size*

Create a small set of new input/output samples that were not included in the original data set after the NN has been trained on all cases. Figure 2 show the feature availability and the dependency of training set in the feature density. This is a common method for validating the results. Using the new outputs, also known as test set performance metrics, as inputs and the model developed during the training phase, the NN then calculates the pertinent design parameters. The predicted NN outputs are then re-fed into the circuit simulator to produce the predicted performance metrics.

Fig. 3 *Accuracy of the result obtained*

The accuracy of the results is summarized in Figure 3. We can assess the accuracy of the results by computing the average relative error of all test cases after comparing the

performance of the original test set with the predicted performance of each metric. Since all earlier studies focused on circuits that were very similar to each other, a theoretical comparison of the computed joint requirements is helpful [23,24,25]. Reinforcement learning (RL), a subfield of machine learning, trains agents to perform specific tasks by using rewards and penalties. RL does not require training on a labelled data set, in contrast to supervised learning. Making predictions and receiving rewards for those predictions acts as a training process. Depending on how accurately a prediction is made, rewards should be given. Learning a tactic that maximizes the overall reward is the aim of the training phase [26]. The use of RL in the creation of IC is still not very common. It is important to mention the fundamentals of RL in IC design before getting into the specifics [27]. As a vector of performance, the state of the circuit is represented. The RL agent uses this vector as input, modifies the values of the design parameters to take actions, computes the rewards, and, if the rewards rise, switches to new states.

Conclusion

Offline optimization of the neuronal networks' weights and biases was carried out using gradient descent and an n-dimensional objective function. Base Neuron's hardware architecture was constructed using its 1 point 2-micron CMOS operational amplifiers. The best pattern recognition results were achieved by applications made with straightforward neuron circuits. An efficiency of 96% was displayed by the MLP architecture. Although might already exist, additional applications must wait for development. Future research will focus on creating and utilizing neural network circuits that optimize objective functions. The findings of this work can be replicated using a variety of tools, including Verilog AMS and VHDL AMS. Future research will test additional metaheuristic optimization methods to enhance ANN training outcomes. Although we think the proposed technique has been used in the best way possible, it should not rule out the possibility of using another metaheuristic technique in the near future. Although the speed of implementation may be a drawback, this is counterbalanced by the fact that we use a design that only includes the resources that are absolutely necessary for the application.

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