# Comparative Analysis of GDI and CMOS Logic for Low Power VLSI Design: A Case Study on 4-bit Hamming Code Encoder and Decoder

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**Abstract:**

This Paper presents an in-depth analysis of Gate Diffusion Input (GDI) and Complementary Metal-Oxide-Semiconductor (CMOS) logic types in the context of designing a 4-bit Hamming code encoder and decoder. The Project focuses on simulations conducted using Gpdk 250 nm technology to evaluate power consumption, latency, and transistor count. The results demonstrate that GDI logic offers significant advantages over CMOS logic, including nearly 50% power savings, reduced latency, and fewer transistors. These findings highlight the potential of GDI logic as a superior low power design choice for VLSI circuit designers.

Keywords: PMOS, NMOS, VLSI, CMOS, GDI, Hamming code, Encoder, Decoder

## 1. Introduction:

The goal of error-free data communication in digital systems has led to the development of robust error detection and repair algorithms. What sets Hamming codes apart from the rest is their ability to detect and correct single-bit errors in transmitted data. When combined with Gate Diffusion Input (GDI) logic, Hamming codes offer a dependable and efficient way to ensure data integrity in communication systems.

GDI logic, being well-known for its compactness and energy efficiency, enables the design of encoders and decoders for the Hamming code. By applying the ideas of GDI logic, designers can create compact, power-efficient circuits that encode and decode data and have integrated error detection and repair.

This brief introduction looks at the connection between Hamming codes and GDI logic and demonstrates how GDI-based designs can increase the reliability and efficiency of data communication systems. By integrating GDI logic, hamming code encoders and decoders can offer robust error detection and correcting procedures, enabling error-free data transport in a range of digital communication applications.

## 2. GATE DIFFUSION INPUT (GDI) TECHNIQUE

Gate Diffusion Input (GDI) is a digital logic style that is used to implement Boolean functions in integrated circuits. It is known for its simplicity, reduced transistor count, and potential for low-power consumption.

The GDI (Gate Diffusion Input) logic cell, which has four terminals—Inputs G, P, and N—as well as an output (Y), is shown in Figure 1. The N-MOS and P-MOS transistors share a same gate in the gate input (G). Similar to the VDD connection in a typical CMOS inverter, the input P is connected to the source of the P-MOS transistor. Like the ground connection in a CMOS inverter, the input N of the N-MOS transistor is connected to its source. The transistors' common drain terminal is where the output Y is obtained.

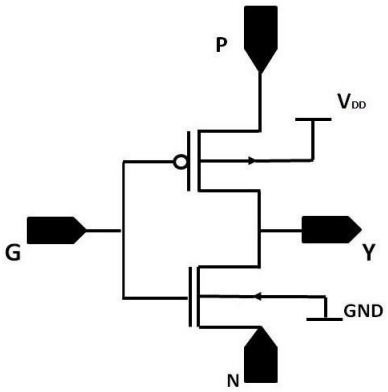



**Figure 1:** Basic GDI cell

**Table1**: GDI, CMOS, and PTL design methodologies used to AND and OR cells.

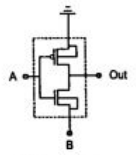
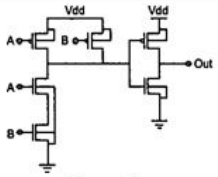
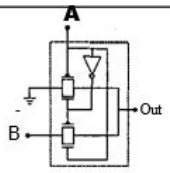
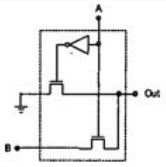
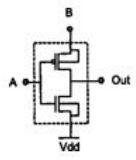
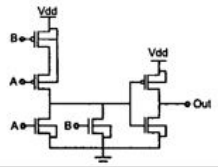
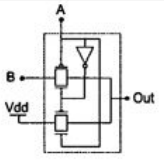
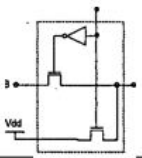
| | GDI | CMOS | TC | N-PG |
|---|---|---|---|---|
| AND |  |  |  |  |
| | 2 transistors | 6 transistors | 6 transistors | 4 transistors |
| OR |  |  |  |  |
| | 2 transistors | 6 transistors | 6 transistors | 4 transistors |

**Table2**: Different GDI Cell-Based Logic Functions and Their Input Combinations

| Basic functions using GDI Cell | | | | | No. of transistors | |
|---|---|---|---|---|---|---|
| G | P | N | FUNC | OUTPUT | GDI | CMOS |
| A | B | 1 | OR | A+B | 2 | 6 |
| A | 0 | B | AND | A.B | 2 | 6 |
| A | B | C | MUX | $\bar{A}.B + A.C$ | 2 | 12 |
| A | B | $\bar{A}$ | XOR | $\bar{A}.B + A.\bar{B}$ | 4 | 16 |
| A | 1 | 0 | INV | $\bar{A}$ | 2 | 2 |

### 3. Generation of Hamming Code

The Hamming code is a method for generating error-correcting codes that can detect and correct single-bit errors in transmitted data. Here is a concise explanation of how to generate Hamming code:

The key steps are:

i. Compute the required number of redundant/parity bits (r) and data bits (m). It is related as follows: 2^r ≥ m + r + 1. For instance, r = 4 redundant bits are required if there are 7 data bits.
ii. Empty the parity bit locations and allocate the data bits to certain codeword locations. The positions of the parity bits are powers of two, such as 1, 2, 4, 8, etc.
iii. Determine the parity bit positions and then compute the parity bits by comparing the parities of the bits in the respective patterns:
iv. Parity bit 1 verifies that bits at places 1, 3, 5, 7, and so on are in parity.
v. Parity bit 2 verifies the bits at places 2, 3, 6, 7, and so on are in parity.
vi. Parity bit 4 verifies the bits in places 4–7, 12–15, and so on are in parity.
vii. For the remaining parity bits, continue as before.
viii. To make the parity of the checked bits even, set each parity bit to 0 or 1.
ix. Because the generated codeword includes both the calculated parity bits and the original data bits, single-bit errors can be found and fixed.

**Table 3**: Shows the Formation of Hamming Code

| Hamming code bit position | $H_1$ | $H_2$ | $H_3$ | $H_4$ | $H_5$ | $H_6$ | $H_7$ |
|---|---|---|---|---|---|---|---|
| Type of data bit | $P_1$ | $P_2$ | $D_1$ | $P_3$ | $D_2$ | $D_3$ | $D_4$ |

### 3.1 Hamming code Encoder

XOR gates can be used to implement the architecture of the Hamming code encoder (either for even parity or odd parity). The construction of the Hamming code encoder is shown in the Figure 2.

**Figure 2**: Hamming Code Encoder



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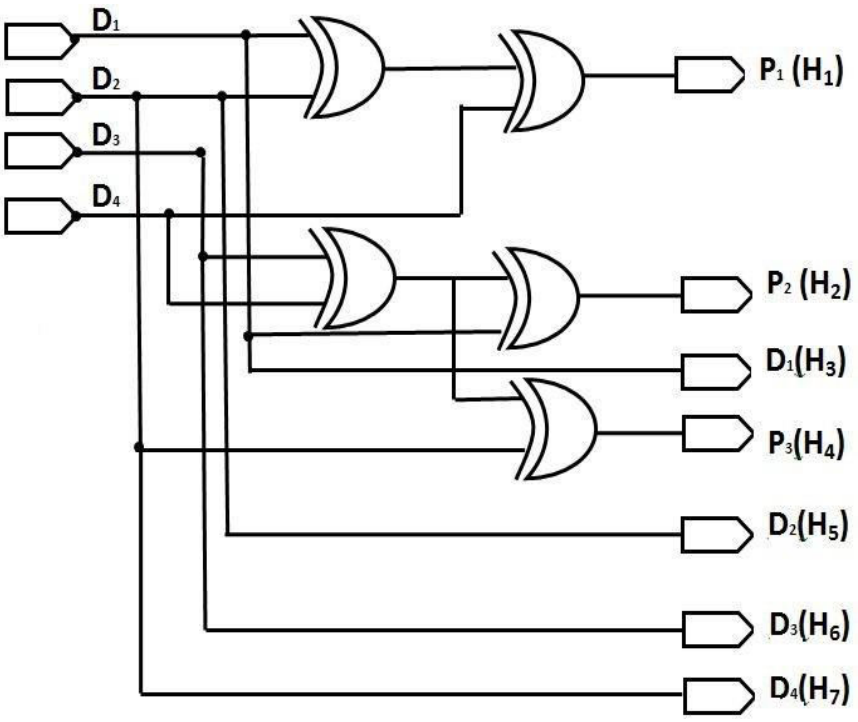
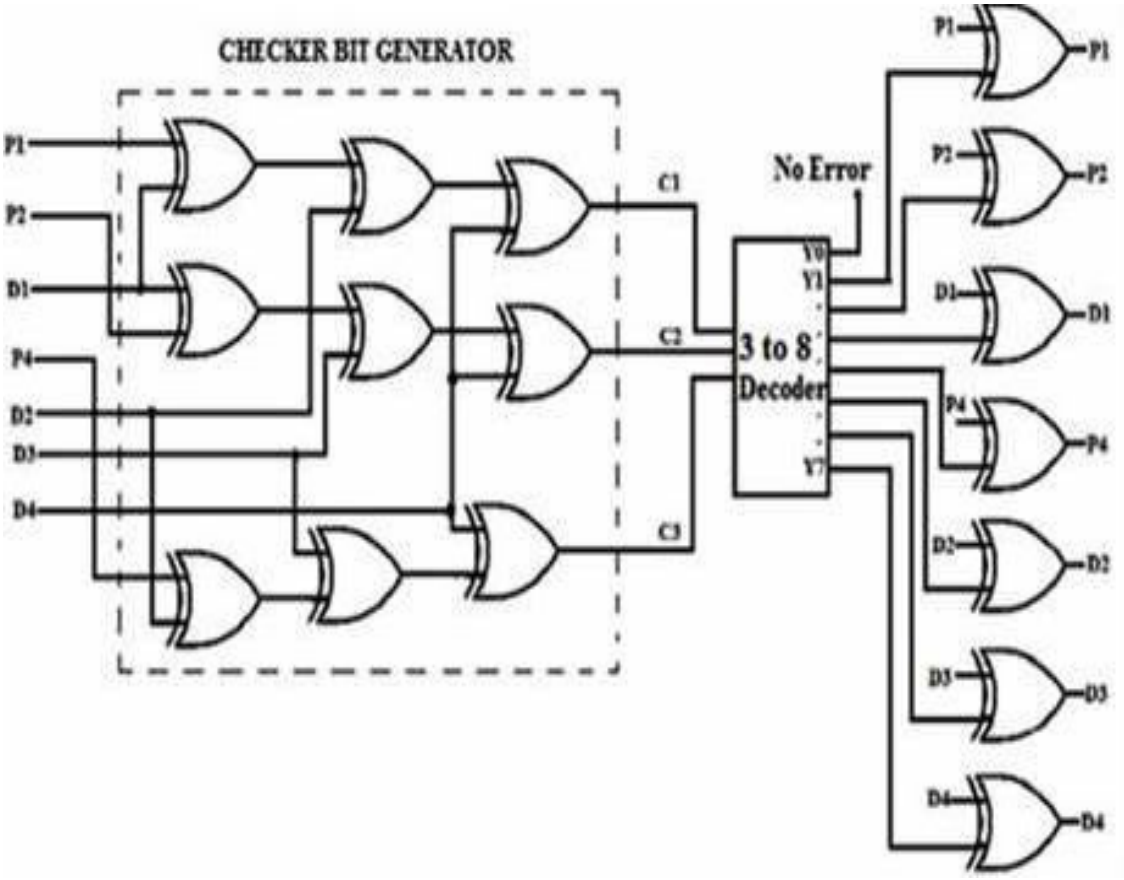



### 3.2 Hamming Code Decoder

A Hamming code decoder is used at the receiving end of digital data transfer to decode data packets and fix any errors. The code word produced by the encoder circuit is conveyed through the transmission media during data transmission. When the decoder receives the code word, it looks for mistakes.

There are two steps in the decoding process. Using a check bit generator that functions similarly to the encoder, the decoder first creates check bits to confirm the parity of the data it has received. In the second phase, the decoder uses a 3-to-8 decoder to locate the error bit locations and de-multiplexers to fix them if the check bit generator finds any mistakes. The Hamming code decoder's architecture is depicted in Figure 3.

**Figure 3:** Hamming Code Decoder


CHECKER BIT GENERATOR
P1
P2
D1
P4
D2
D3
D4
C1
C2
C3
No Error
3 to 8
Decoder
Y0
Y1
Y7
P1
P2
D1
P4
D2
D3
D4

## 4. Simulation Results:

### 4.1 Design and Simulation Results of CMOS OR Gate

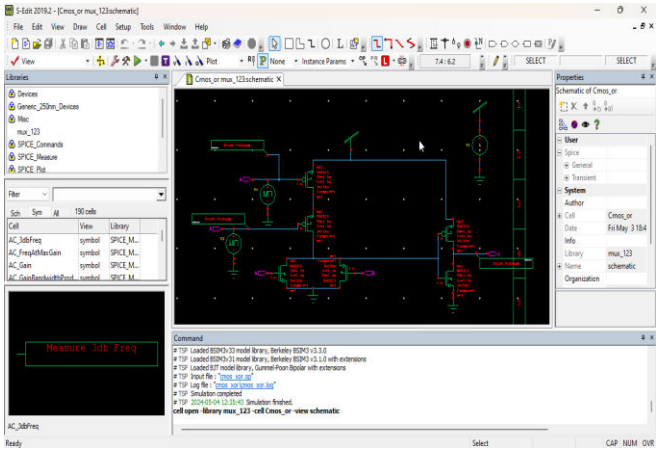


Figure 4: Design of CMOS OR Gate

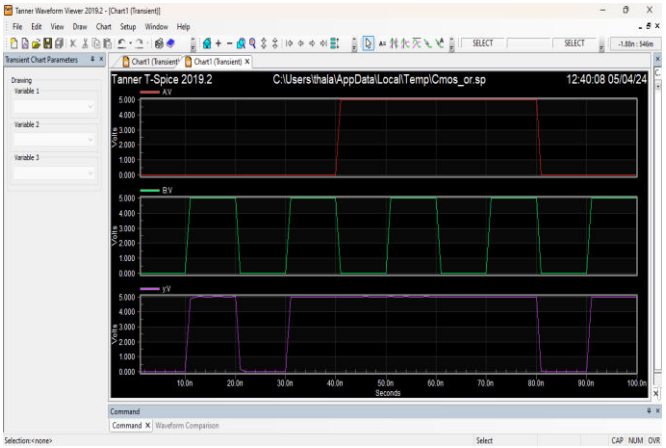


Figure 5: Output waveforms of CMOS OR Gate

### 4.2 Design and Simulation Results of GDI OR Gate

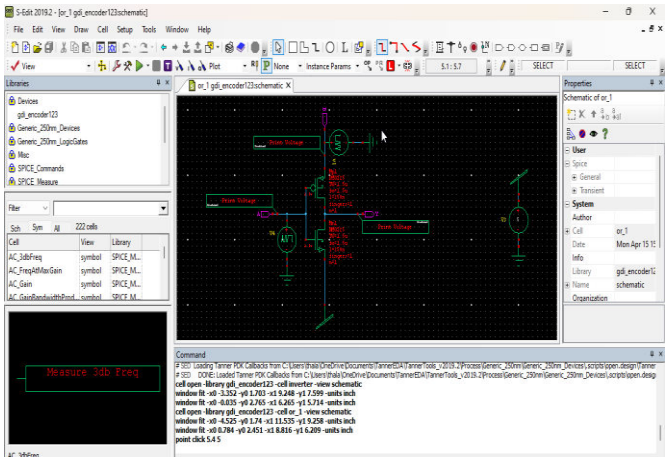


Figure 6: Design of GDI OR Gate

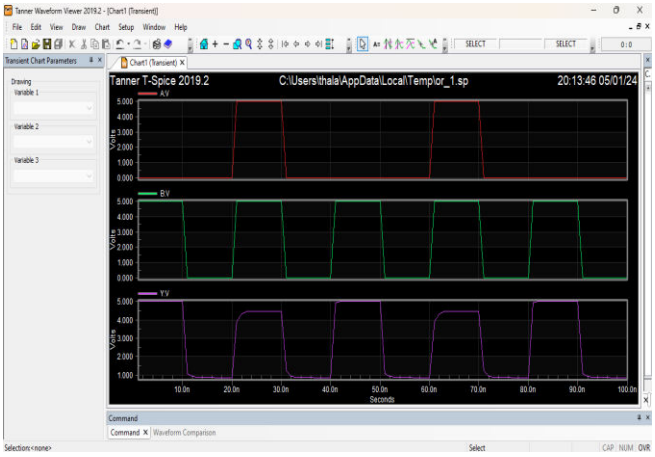


Figure 7: Output Waveforms of OR Gate

**Table 4**: Message Bits Transmission at Encoder Side

| **Hamming code bit** | **H1** | **H2** | **H3** | **H4** | **H5** | **H6** | **H7** |
|---|---|---|---|---|---|---|---|
| **position Type of data bit** | P1 | P2 | D1 | P3 | D2 | D3 | D4 |
| **Message bits for transmission** | **0** | **1** | **1** | **0** | **0** | **1** | **1** |

### 4.3 Design and Simulation Results of GDI Encoder

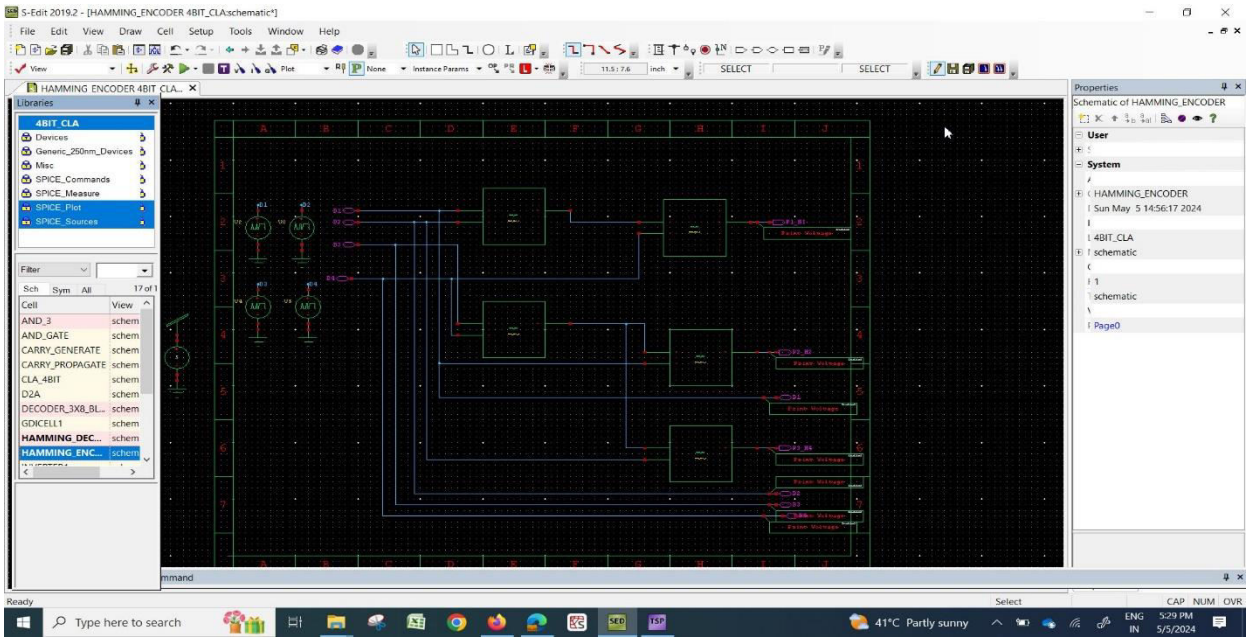



Figure 8: Hamming Code Encoder using GDI logic

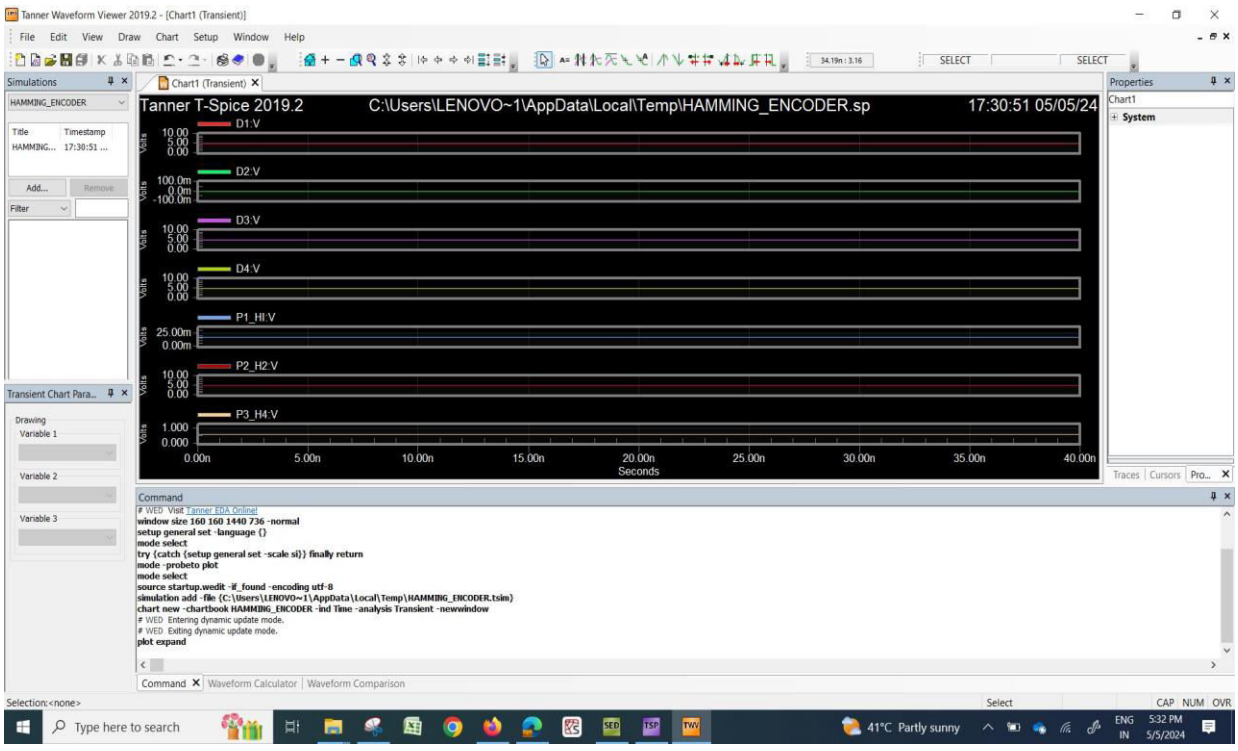



Figure 9: Hamming Code Encoder output waveforms

### 4.4 Design and Simulation Results of GDI Decoder

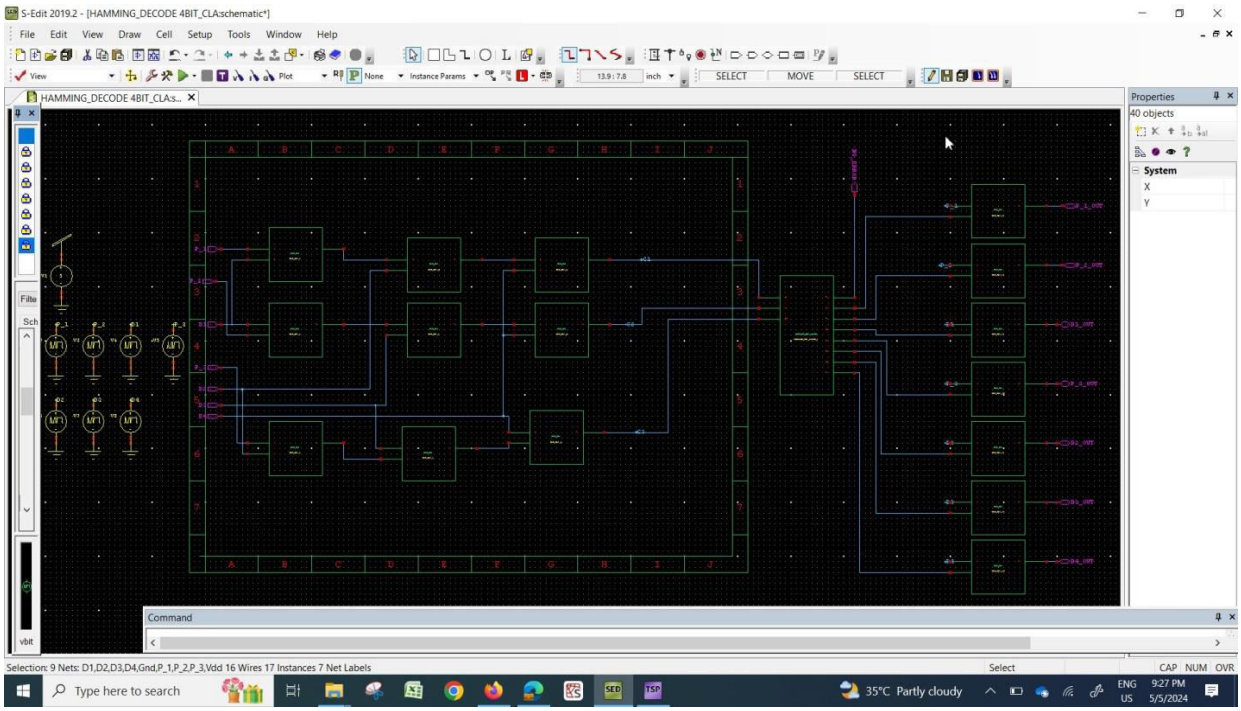



Figure 10: Design of Hamming Code Decoder circuit

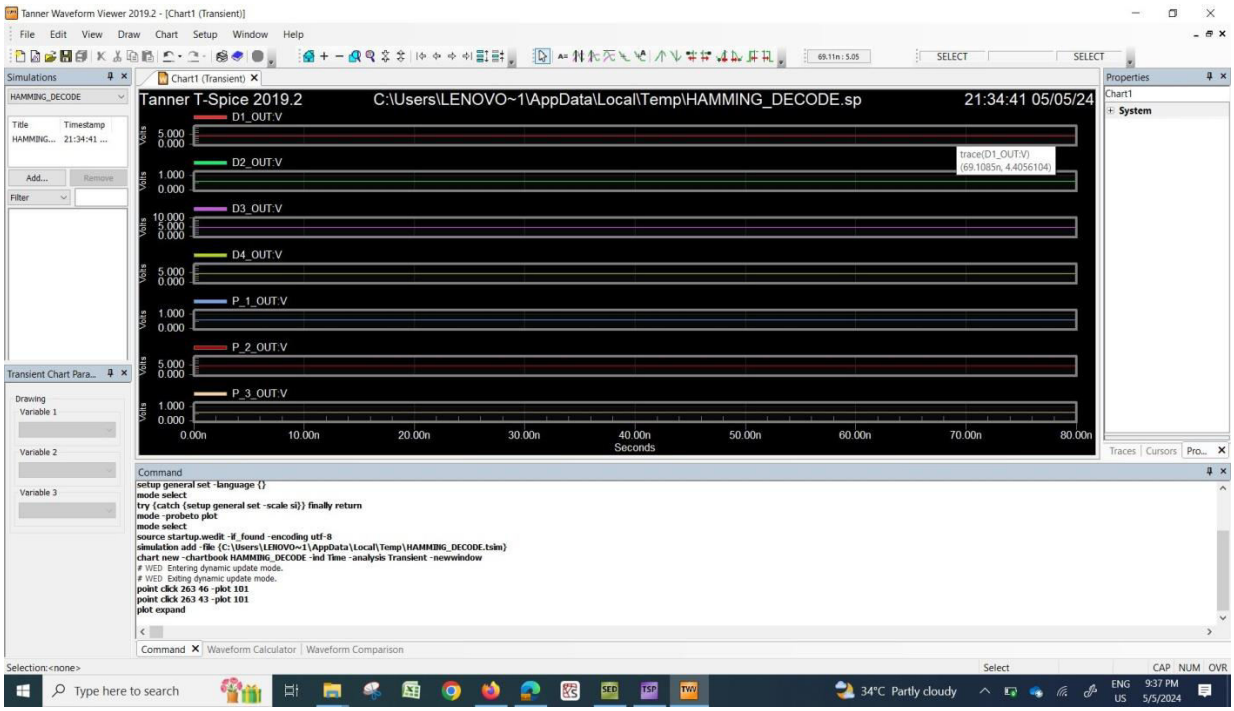



Figure 11: Output Waveforms of Hamming Code Decoder Circuit

**Table 4**: Message Bits Transmission at Encoder Side with Single bit error and Received data at Decode side without error.

| **Hamming code bit** | **H1** | **H2** | **H3** | **H4** | **H5** | **H6** | **H7** |
|---|---|---|---|---|---|---|---|
| **position Type of data bit** | P1 | P2 | D1 | P3 | D2 | D3 | D4 |
| **Message bits for transmission** | **0** | **1** | **1** | **0** | **0** | **1** | **1** |
| **Message bits for transmission with Error at Encoder Side** | **0** | **1** | **1** | **0** | **0** | **1** | **0** |
| **Original message Received at Decoder Side without Error** | **0** | **1** | **1** | **0** | **0** | **1** | **1** |

## 5. Conclusion:

In this study, we explored various GDI (Gate Diffusion Input) logic functions designed for low-power VLSI architecture and conducted simulations to compare them with traditional CMOS logic. We specifically focused on designing and simulating a 4-bit Hamming code encoder and decoder using both GDI and CMOS logic types, utilizing Gpdk 250 nm technology for our experiments. The simulation results revealed that GDI logic provides significant advantages over CMOS logic. Notably, GDI achieved nearly 50% power savings compared to CMOS. Moreover, GDI showed a marked improvement in latency and required fewer transistors for performing operations. By simulating Hamming encoder and decoder circuits with both GDI and CMOS logic, we were able to thoroughly evaluate the benefits of the GDI approach.Overall, our findings clearly indicate that GDI logic is a superior choice for VLSI circuit designers seeking low-power design solutions.

## 6. Future Work:

There are a number of intriguing directions for future development in GDI Logic Based Design of Hamming-Code Encoder and Decoder for Error-Free Data Communication. To obtain higher degrees of error detection and repair, researchers should first investigate more complex error correction codes, such as Reed-Solomon or Turbo codes, which go beyond Hamming codes. Moreover, investigating hardware implementations on FPGA or ASIC platforms would make real-time, error-free data transfer applications possible. Throughput and efficiency might be increased by experimenting with techniques like parallel processing, and in areas where energy is limited, it is critical to optimize designs for low power consumption. Fortifying data integrity and including security measures can strengthen it

against malevolent assaults and improve fault tolerance. Practical effectiveness requires interdisciplinary collaboration for cross-layer optimization and design validation in real-world deployments. Lastly, dynamically modifying encoding and decoding algorithms in response to channel conditions and data patterns might be achieved by using machine learning approaches for adaptive error correction. Together, these approaches seek to further the frontiers of error-free data transfer by utilizing Hamming codes and GDI logic design concepts for improved dependability and performance.

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