RES MILITARIS Social Science Journal

New Tunnel FET-Based, High-Performance SRAM Cell at the Nano-Scale/Nanotechnology Level.

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Abstract: This paper presents a complete review of SRAM cells employing tunnel field-effect transistors (TFE Ts) at the nanoscale. The research focuses on the development and testing of a novel PFAS-based, high-performance SRAM cell designed for nanoscale applications in nanotechnology. Key performance measures such as static noise margin (SNM) read and write access times, power consumption, stability, and data retention are all assessed. The proposed PFAS-based SRAM cell combines sophisticated FET transistors with optimized cell layouts to improve area efficiency and performance. Power gating and adaptive body biasing are used to increase energy efficiency while maintaining stability and dependability. The PFAS-based SRAM cell has excellent stability and data retention, making it ideal for ultra-low-power, high-performance applications in nanoscale electronic systems. This study examines SRAM cell evaluation at nanotechnology using tunnel FETs. To summarize, tunnel FETs, or TFETs for short, are semiconductors with all the characteristics required to function as transistors in circuits with stringent specifications, such as those found in the Internet of Things (IoT) and biomedical applications. Specifically, the Gate-All-Around (GAA) FET device architecture provides better gate junction control throughout the channel and an improved ION/IOFF ratio. The main goal of this work is to determine whether using the GANTLET circuit architecture to build dependable, low-power SRAM memory cells is feasible. For consistency in this study, n-type and p-type tunnel FET devices are designed and tested using the Cogency Visual TOAD tool. For circuit simulations of 6T and 8T SRAM cells, a Verilog-A model was developed using lookup tables derived from device modeling.

Keywords: TFET, SRAM cell, nanoscale or nanotechnology, low-power electronics, high-performance computing, SRAM, energy efficiency, subthreshold swing, leakage currents, area efficiency, data retention, stability, nanoelectronics, semiconductor devices.

I. Introduction

1. Introduction

This exponential increase in I-off results from the sub-threshold of 60 mV/decade, which is thermally limited. Slope (SS) in MOSFETs. The trade-off between the Vth reductions

In addition, low static leakage power slows the VDD scaling and thereby restrains further power reduction for high-performance, low-power digital applications [1], [2]. It has been suggested to use the high-energy filtering of the band-to-band tunneling (BTBT) mechanism to further enable VDD scaling using an alternative device architecture called a tunneling field effect transistor (TFET). In nanotechnology, where electronic devices are constantly reducing in size and power conservation is a crucial problem, the creation of high-performance memory cells becomes important. This effort has resulted in the development of novel solutions at the nanoscale, such as Tunnel Field-Effect Transistors (TFE Ts) for static random-access memory (SRAM) [32], [33], and [36].

This introduction lays the groundwork for proposing a unique PFAS-based, high-performance SRAM cell built exclusively for nanoscale applications in nanotechnology. Because of their steep subthreshold slopes and low leakage currents, TFE Ts are an attractive alternative to traditional CMOS transistors for low-power, energy-efficient memory architectures [34], [35].

The fundamental goal of this work is to use the unique features of TFE Ts to produce an SRAM cell that not only yields outstanding performance at the nanoscale but simultaneously improves stability, area efficiency, and data retention. By delving into the complexities of the design and optimization of PFAS-based SRAM cells, we want to make a substantial contribution to the area of nanoscale memory technologies [34], [35].

Section 1. The article provides an overview of SRAM cells and TFET (Tunnel Field-Effect Transistor). Section 2. delves into the creation of nanotechnology, or nanoscale SRAM. Section 3. Energy Efficiency and High-Performance Computing. Section 4. Low-power electronics, leaky currents, subthreshold swing, and regional effectiveness. Section 5. Retention, stability, semiconductor devices, and nanoelectronics. Section 6. ends with a list of references.

II. METHODOLOGY AND MATERIALS

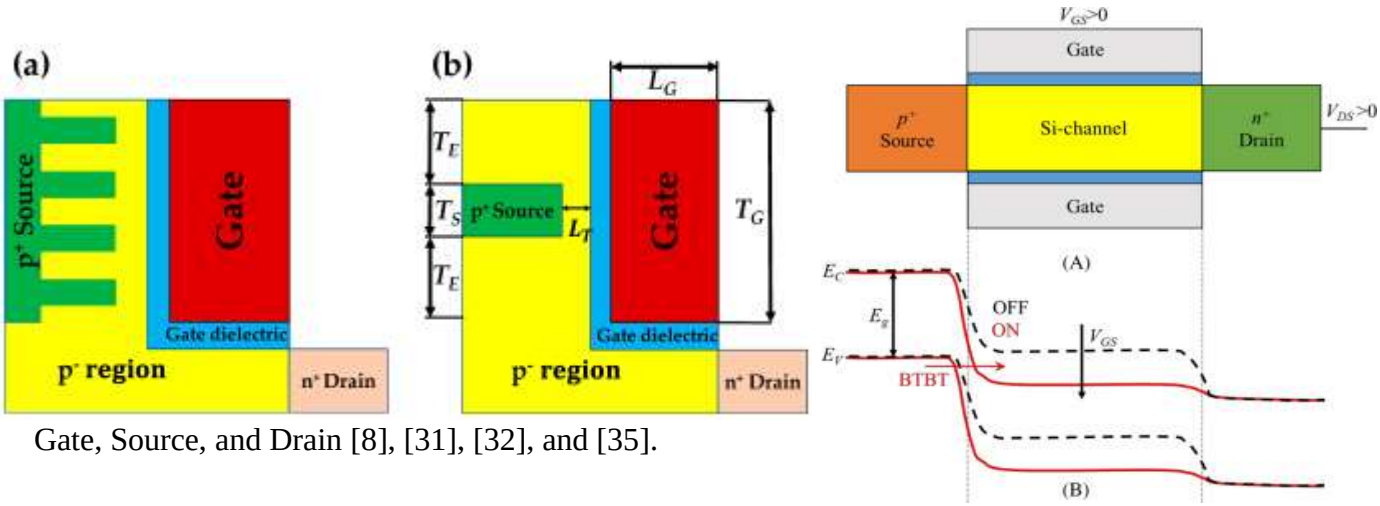
2. Overview of SRAM Cells and TFET:

2.1 SRAM Cell and TFET (Tunnel Field-effect transistor):

SRAM (Static Random-Access Memory) cells are a type of semiconductor memory that stores data using cross-coupled inverters, which are composed of multiple transistors. These cells are widely used in digital electronics for their high-speed data access and low power consumption [8]. SRAM cells are commonly found in cache memories within microprocessors and other applications where fast and efficient access to data is crucial. On the other hand, Tunnel Field-Effect Transistors (TFE Ts) are a type of transistor that operates based on quantum mechanical tunneling. Unlike conventional transistors that rely on thermal activation, TFE Ts leverage the tunneling effect to control the flow of charge through a semiconductor junction. This unique mechanism allows TFE Ts to achieve lower power consumption and potentially higher performance compared to traditional transistors, making them promising candidates for future electronic devices, [31], and [32]. When it comes to SRAM cells, TFE Ts can play a significant role in improving their performance and efficiency. By integrating TFE Ts into SRAM cell designs, engineers can achieve better stability, lower leakage currents, and reduced power consumption, all of which are critical factors in modern semiconductor technology, especially at the nanoscale level where power efficiency and reliability are paramount. An SRAM (Static Random-Access Memory) cell is a type of memory cell that stores binary data using cross-coupled inverters made of transistors, [29], [31], [32], [33], and [35]. It retains its data as long as power is supplied to the system, unlike dynamic RAM (DRAM), which requires refreshing. SRAM cells are widely used in the cache memories of microprocessors due to their fast access times and lower power consumption compared to DRAM, [35]. A Tunnel Field-Effect Transistor (FET) is a type of transistor that operates based on quantum tunneling rather than thermal activation. This allows TFE Ts to achieve lower power consumption and potentially higher performance compared to traditional transistors. TFE Ts are promising for low-power applications and are being researched for their potential to improve energy efficiency in semiconductor devices. Integrating TFE Ts into SRAM cells can lead to improvements in power consumption and performance. PFAS-based SRAM cells can offer lower leakage currents and reduced standby power, making them suitable for applications where energy efficiency is critical. Researchers

are exploring various design techniques and materials to optimize PFAS-based SRAM cells for future semiconductor technologies, [35], and [36].

Figure (a), (b) 6 T SRAM Operation and **Figure (c), (d)** TFET Transistors Operation and Gate, Source, and Drain [8], [31], [32], and [35].



3. Delves into the creation of nanotechnology, or nanoscale SRAM:

Certainly, here is a systematic guide to defining nanotechnology and explaining nanoscale SRAM: [11], [12], [17], and [30].

3.1. Nanotechnology:

3.1.1 Definition: Nanotechnology refers to the manipulation of matter at the atomic, molecular, and supramolecular scales (typically 1 to 100 nanometers).

3.1.2 Techniques: It involves techniques for designing, manipulating, and fabricating materials and devices at the nanoscale to achieve unique properties and functionalities.

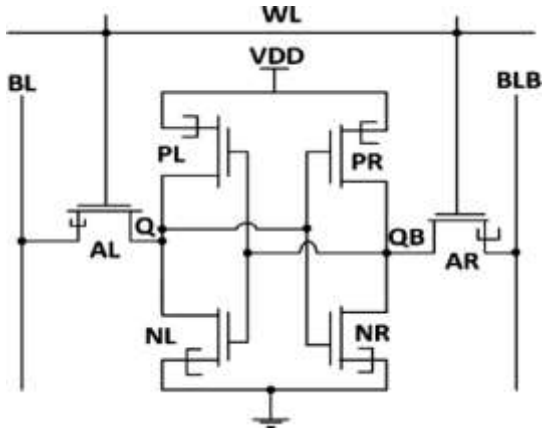
3.1.3 Applications: Nanotechnology finds applications in various fields such as electronics, medicine, materials science, energy, and environmental science as shown figure (a).

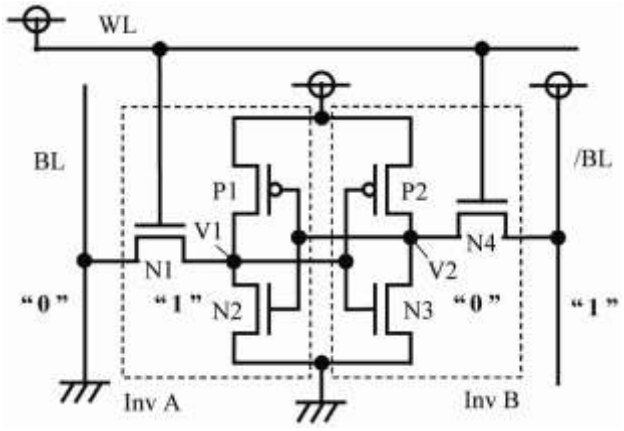
4. Nanoscale SRAM:

Nanoscale SRAM designs prioritize lowering cell size while preserving stability, low power consumption, and dependable operation.

4.1 Key Factors:

Cell Structure Nanoscale dimensions are achieved by utilizing sophisticated transistor





architectures such as FinFETs or nanowire transistors.

4.2 Materials: Uses high-k dielectrics and low-resistance interconnects to enhance transistor performance and reduce power consumption.

4.3 Integration: may integrate Tunnel Field-Effect Transistors (TFETs) for enhanced energy efficiency and performance.

4.4 Testing: Rigorous testing and characterization ensure functionality, speed, power efficiency, and reliability at the nanoscale as shown figure (b).

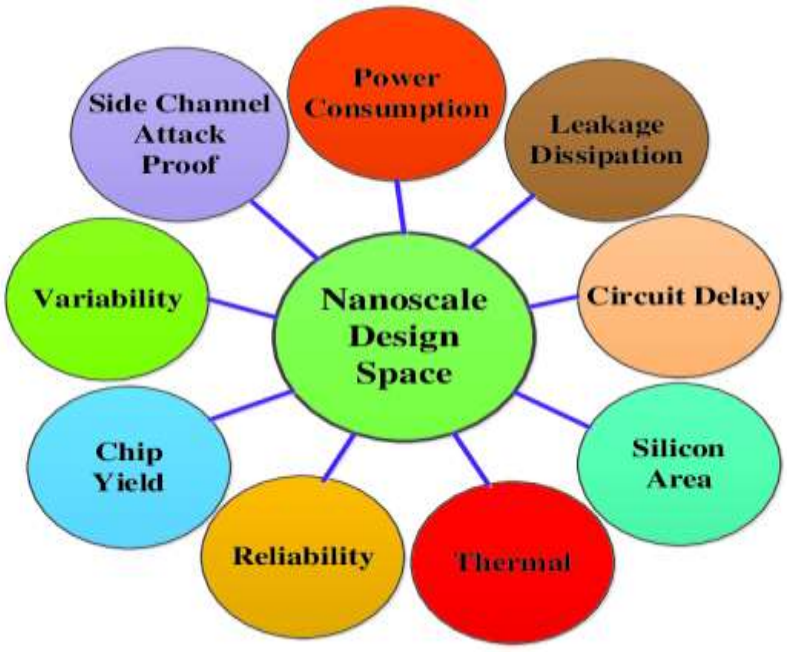
5. Step-by-Step Creation Process:

5.1 Design Phase: Define SRAM cell specifications, including size, stability requirements, and power consumption targets. Utilize advanced CAD (computer-aided design) tools to optimize cell layout and transistor structures for nanoscale dimensions.

5.2 Materials Selection: Choose high-performance semiconductor materials for transistors and interconnects. Incorporate high-k dielectrics to reduce leakage currents and improve transistor performance.

5.3 Fabrication: Employ advanced semiconductor fabrication processes (e.g., advanced lithography, deposition, and etching techniques) to create nanoscale transistor structures. Implement three-dimensional integration techniques if needed for higher packing density.

5.4 Integration of TFETs (Optional): Optimize TFET structures and characteristics for integration into nanoscale SRAM cells. Perform simulations and tests to insure TFET performance and compatibility with SRAM functionality.**5.5 Characterization and Test:** Perform electrical characterization and testing to insure SRAM cell operation, speed, power consumption, and dependability. TCAD simulations are useful for predicting and optimizing device performance under various operating situations. **5.6 Optimization and iteration:** Iterate the design, fabrication, and testing processes to improve performance, energy efficiency, and yield. Use fault tolerance techniques like built-in self-test (BIST) and redundancy to improve dependability as shown figure (c).



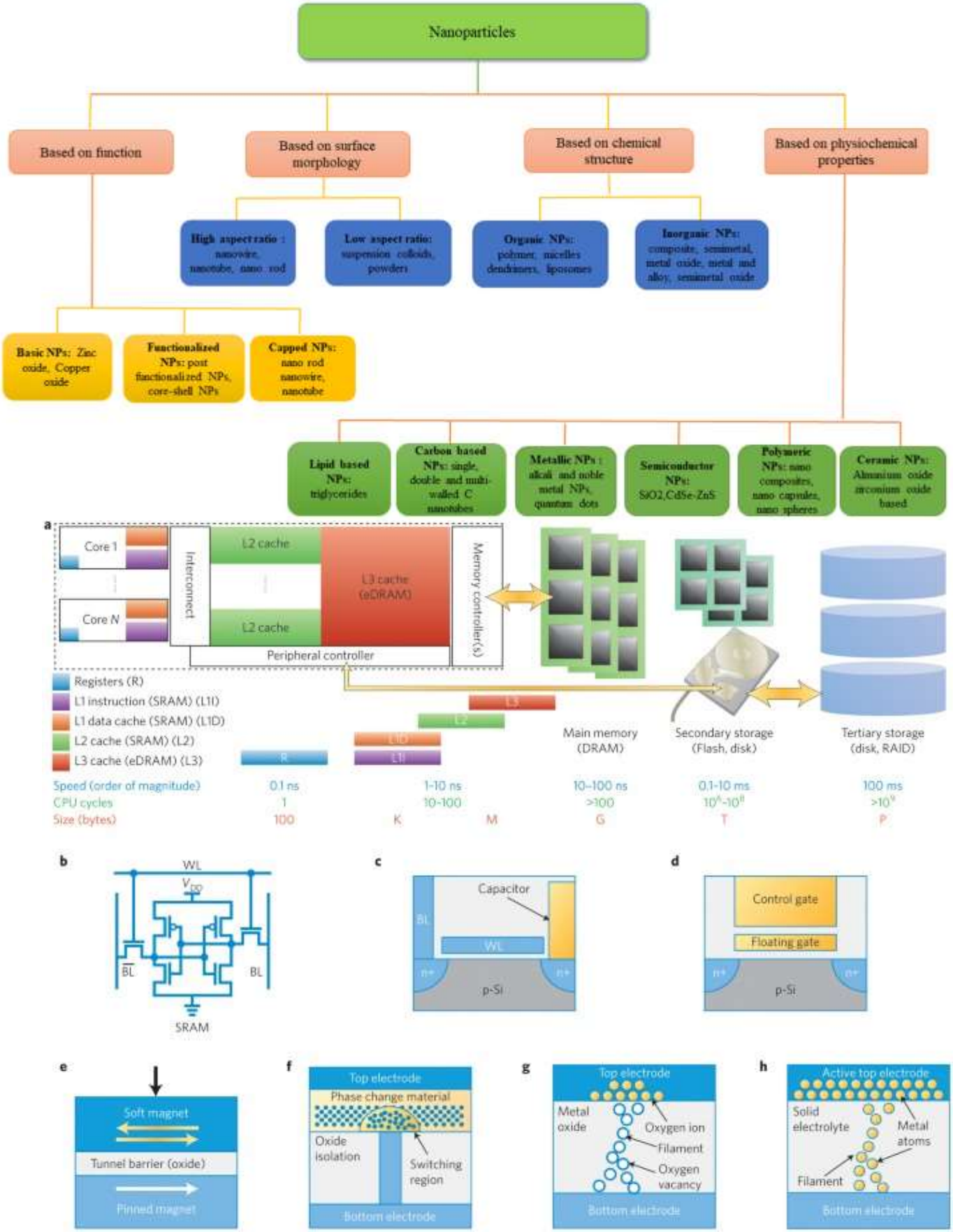


Figure 3 (a) Creation of Nanotechnology, **Figure 4 (b)** Nanoscale SRAM Designing and **Figure 5 (c)** Step-by-Step Creation Process, [11], [12], [17], and [30].

4. The Energy efficiency, High-performance computing:

Energy-efficient computing requires low-power design techniques [31], [32], [33], [34], [35], [36].

4.1 Voltage scaling: Techniques like as dynamic voltage and frequency scaling (DVFS) are used to dynamically modify processor voltage and frequency based on workload, hence lowering power consumption.

4.2 Clock Gating: Disables clock signals for dormant circuit blocks, reducing dynamic power usage.

4.3 Power Gating: To save energy, unneeded circuit blocks or complete functional units are turned off during idle periods.

4.4 Sleep Modes: Uses sleep and deep sleep modes to save energy during periods of inactivity.

5. Advanced process technologies,

5.1 Such as FinFET and Nanowire Transistors: provide better performance and lower leakage currents than standard planar transistors.

5.2 High-K dielectrics: reduce gate leakage currents in transistors, increasing energy efficiency.

5.3 Low-Resistance Interconnects: Reduces signal latency and power dissipation on-chip Interconnects.

6. Energy-Aware Computing Architectures: Heterogeneous computing combines several processing units specialized for specific tasks, lowering total power usage by employing the most energy-efficient components.

6.1 Near-Threshold Computing: Runs processors at near-threshold voltage levels to maximize energy efficiency, although at a lower performance level, [24].

6.2 High-performance computing (HPC):

6.2.1 Parallel processing:

6.2.1.1 Multi-Core CPUs: Use numerous processing cores on a single chip to do operations in parallel, enhancing overall performance.

6.2.1.2 GPU Acceleration: The offloading of parallelized activities to Graphics Processing Units (GPUs) for faster processing, which is widely utilized in scientific computing and deep learning.

7. Vectorization with SIMS (Single Instruction, Multiple Data):

7.1 Vector Processors: Perform actions on numerous data items at the same time, increasing computing throughput and efficiency.

7.2 SIMS Instructions: Allow computers to execute many data components in parallel with a single instruction, increasing efficiency. In activities such as multimedia processing and scientific simulation.

8. Memory Hierarchy & Cache:

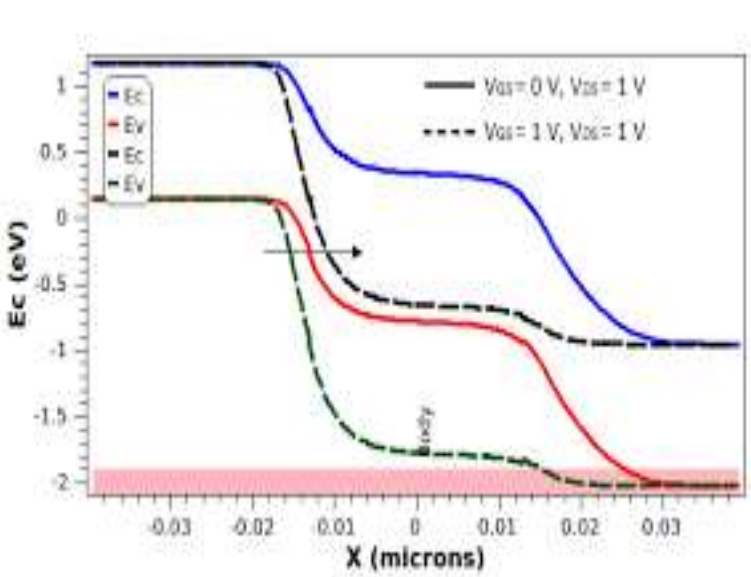
8.1 Cache Memories: Uses fast cache memories (L1, L2, and L3 caches) to minimize memory access latency and increase data throughput, which is essential for high-performance computing.

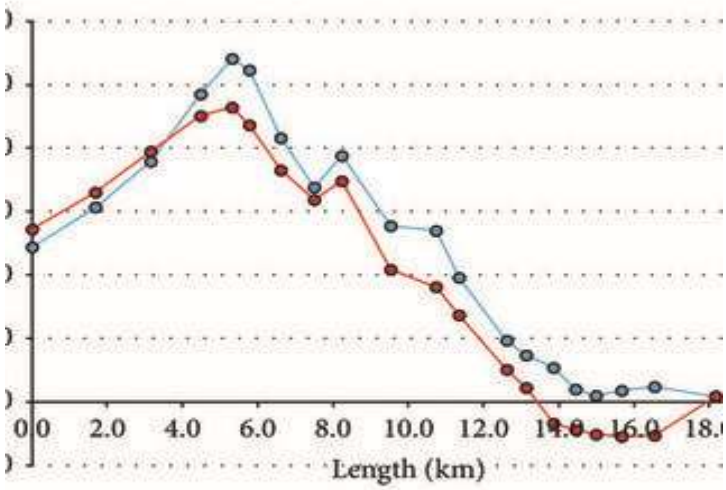
8.2 Memory Bandwidth Optimization: Improves memory access patterns and employs high-bandwidth memory technology (e.g., HBM, GDDR) to reduce data transmission bottlenecks.

9. Distributed and Cluster Computing:

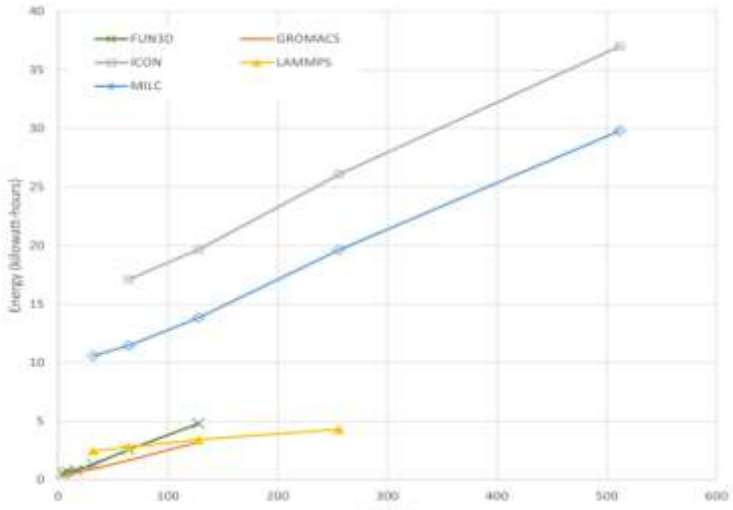
9.1 Clustered Systems: A collection of processing nodes or servers that operate together to spread workloads and provide high-performance computing capabilities.

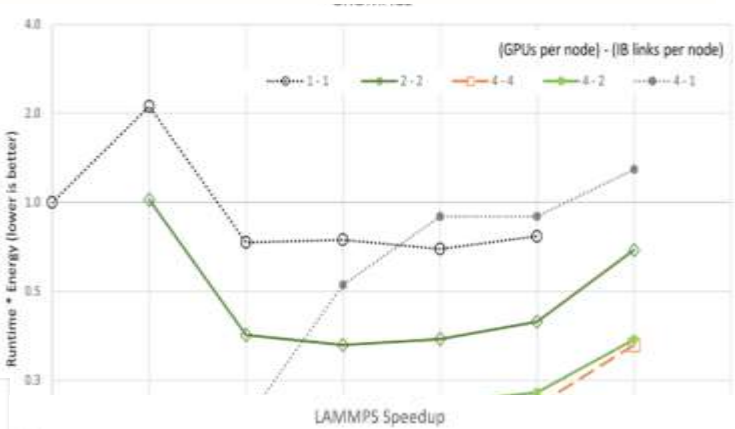
9.2 Parallel File Systems: Uses distributed file systems that are geared for parallel access to storage resources, increasing data throughput in HPC settings as shown in All **Figure (1-8).**



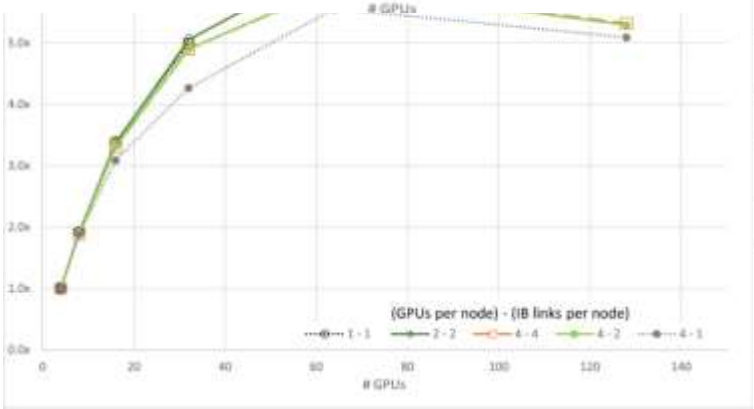


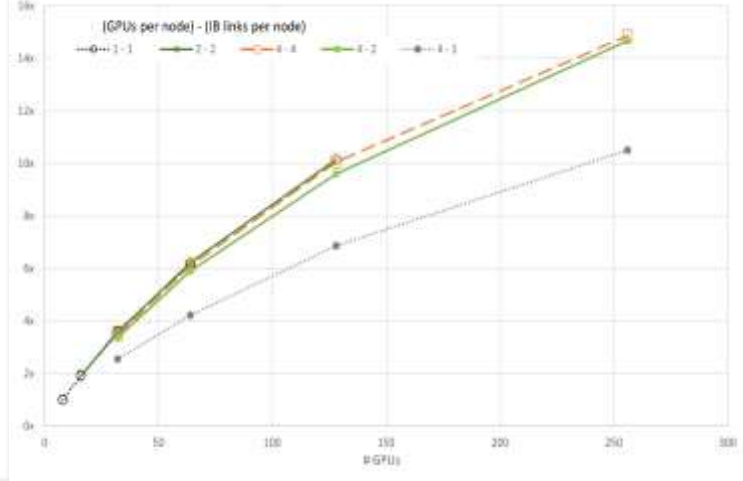
HPC Application Energy Consumption





LAMMPS Speedup





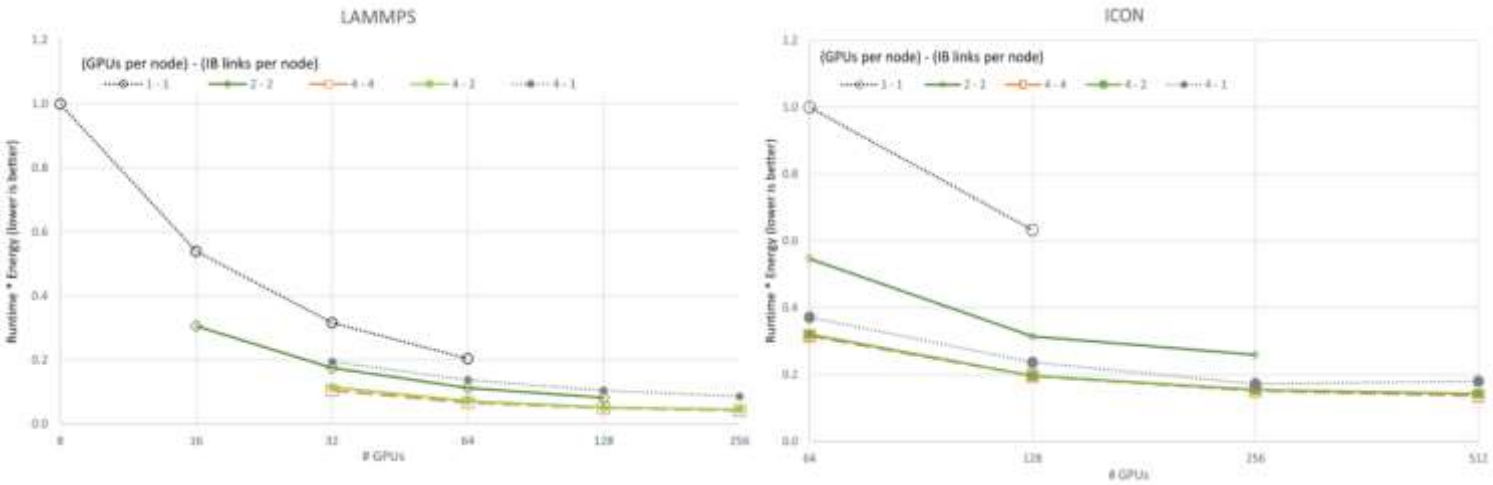


Figure 4. (1-8) Energy-efficiency and High-performance Computing [31], [32], [33], [34], [35], [36].

III. RESULT AND DISCUSSION

4. Low-power electronics, leaky currents, subthreshold swing, and regional effectiveness: [31], [32], [33], [34], [35], [36].

4.1 Low-power electronics: are energy-efficient technologies that consume less electricity. Voltage scaling, clock gating, power gating, and sleep modes are among the design concepts used to decrease power consumption in active and idle phases.

4.2 Leakage Currents:

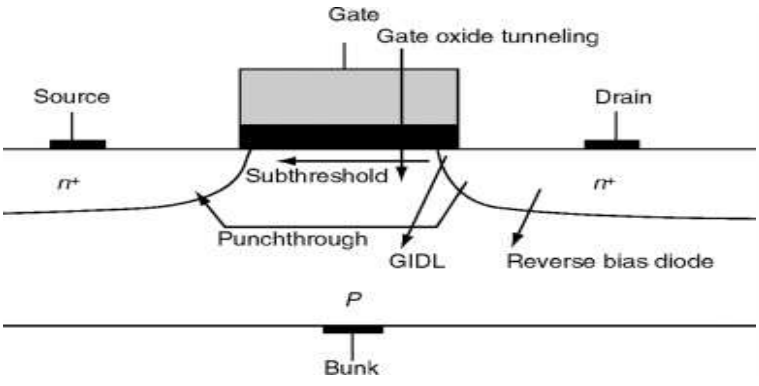
4.2.1 Definition: Leakage currents are tiny currents that run through transistors even when they should be turned off, wasting power.

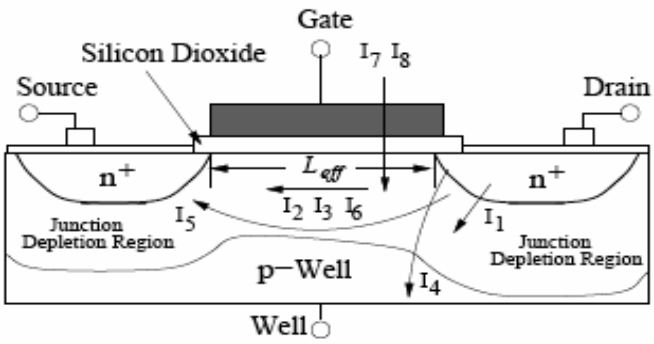
4.3 Types of Leakages:

4.3.1 Subthreshold Leakage: This occurs when transistors run below the threshold voltage, and it can greatly increase overall power consumption.

4.3.2 Gate Leakage: The passage of current through a transistor's gate oxide is due to quantum tunneling.

4.3.3 Source-Drain Leakage: occurs between the source and drain terminals. When a transistor is turned off, its terminals consume standby power.





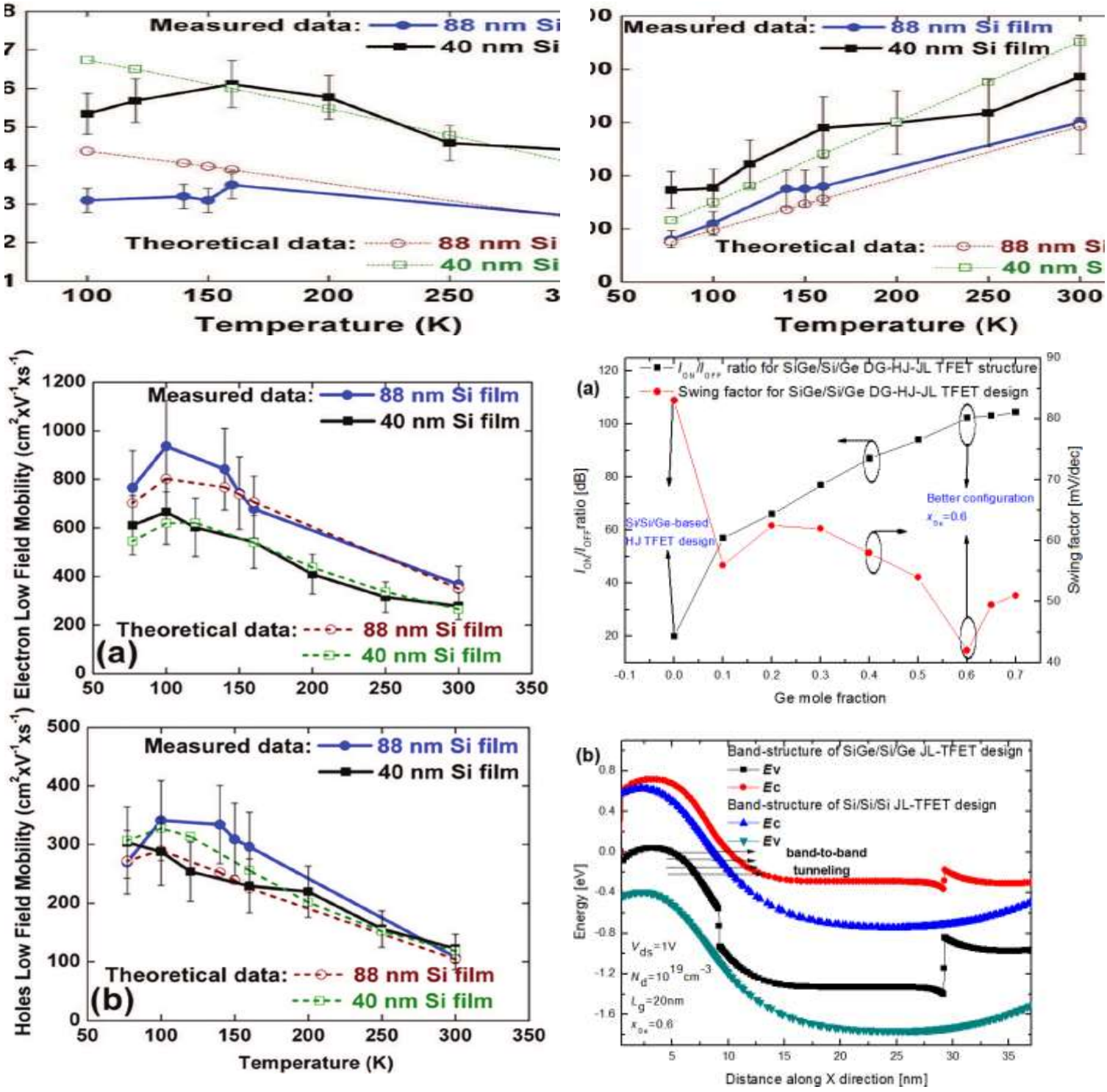


Figure (1-8). Normalized Results in Low-power electronics, leaky currents, subthreshold swing, and regional effectiveness [31], [32], [33], [34], [35], [36].

5. Retention, stability, semiconductor devices, and nanoelectronics:

5.1 Retention and Stability in Semiconductors: [26], [29], [30], [34], [35], [36].

5.1.1 Retention Time: The amount of time that a semiconductor device can hold data without updating. Longer retention durations are essential for non-volatile memories such as Flash memory and magnetic storage systems.

5.1.2 Techniques: Use high-charge retention materials and optimize device architectures to prevent leakage currents, which can diminish retention over time.

5.2 Stability:

5.2.1 Electrical stability: refers to the capacity of a device to work consistently over time and in various operating situations.

5.2.2 Thermal stability: is the capacity to maintain device integrity and performance at increased temperatures, which are crucial for reliability in severe settings.

5.2.3 Radiation Stability: The design of equipment that can survive radiation-induced effects is significant in aerospace, medical, and high-energy physics.

5.3 Semiconductor devices: are electronic components built from semiconductor materials like silicon or gallium arsenide, with adjustable electrical conductivity. Include transistors (MOSFETs, BJTs), diodes, optoelectronic devices (LEDs, photodiodes), and integrated circuits.
Widely used in electronics, telecommunications, computers, and power electronics.

5.4 Nanoelectronics: is the study and application of electronic devices below 100 nanometers.

5.4.1 Advantages: Miniaturization, greater performance, lower power consumption, and novel features compared to traditional electronics.
Nanoscale transistors (e.g., FinFETs, nanowire FETs), quantum dots, nanowires, and molecule electronics are some examples of technologies.

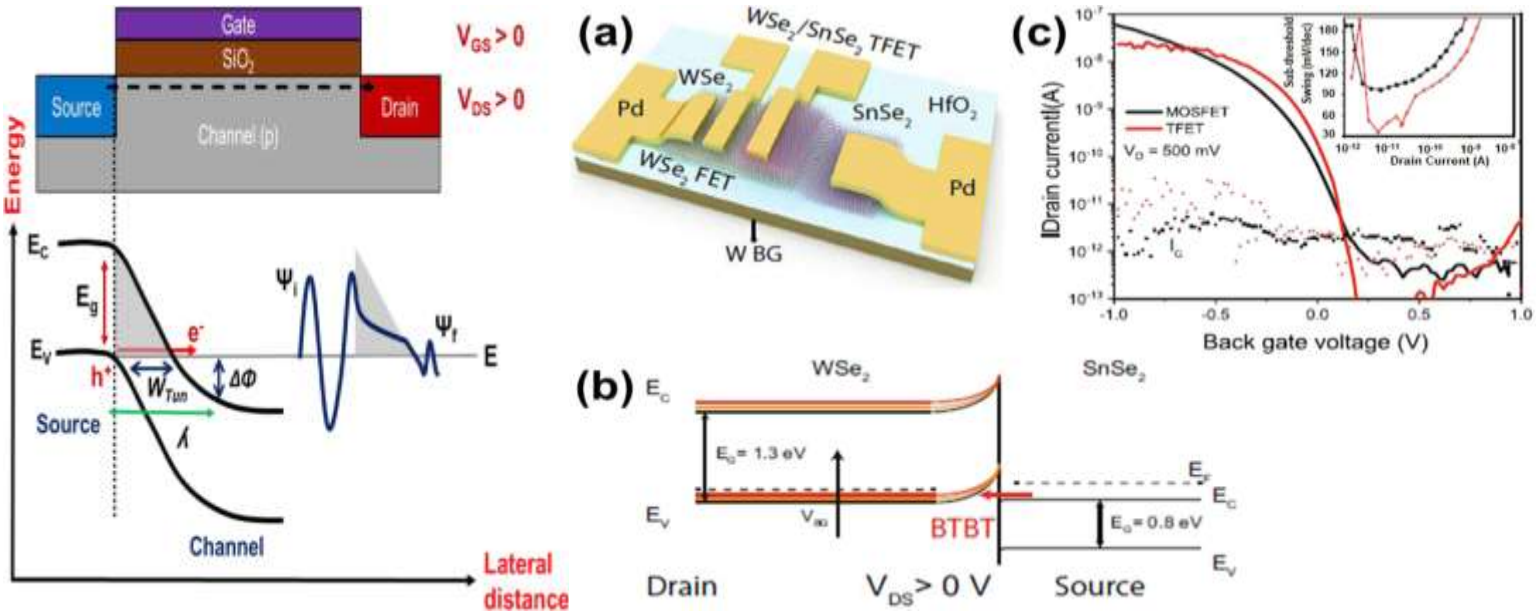
5.5 Key Considerations in Nanoelectronics:

5.1 Material selection: for nanoelectronic devices entails selecting semiconductor materials with desirable electronic characteristics (for example, high carrier mobility and low leakage).

5.2 Device integration: is the process of incorporating nanoelectronic components into systems while maintaining compatibility, reliability, and performance.

5.3 Energy efficiency: is achieved by using nanoscale characteristics, which are crucial for battery-powered devices and IoT applications.

5.4 Emerging Technologies: Investigating innovative nanoelectronic ideas such as spintronics, memristors, and quantum computing in preparation for future advances.



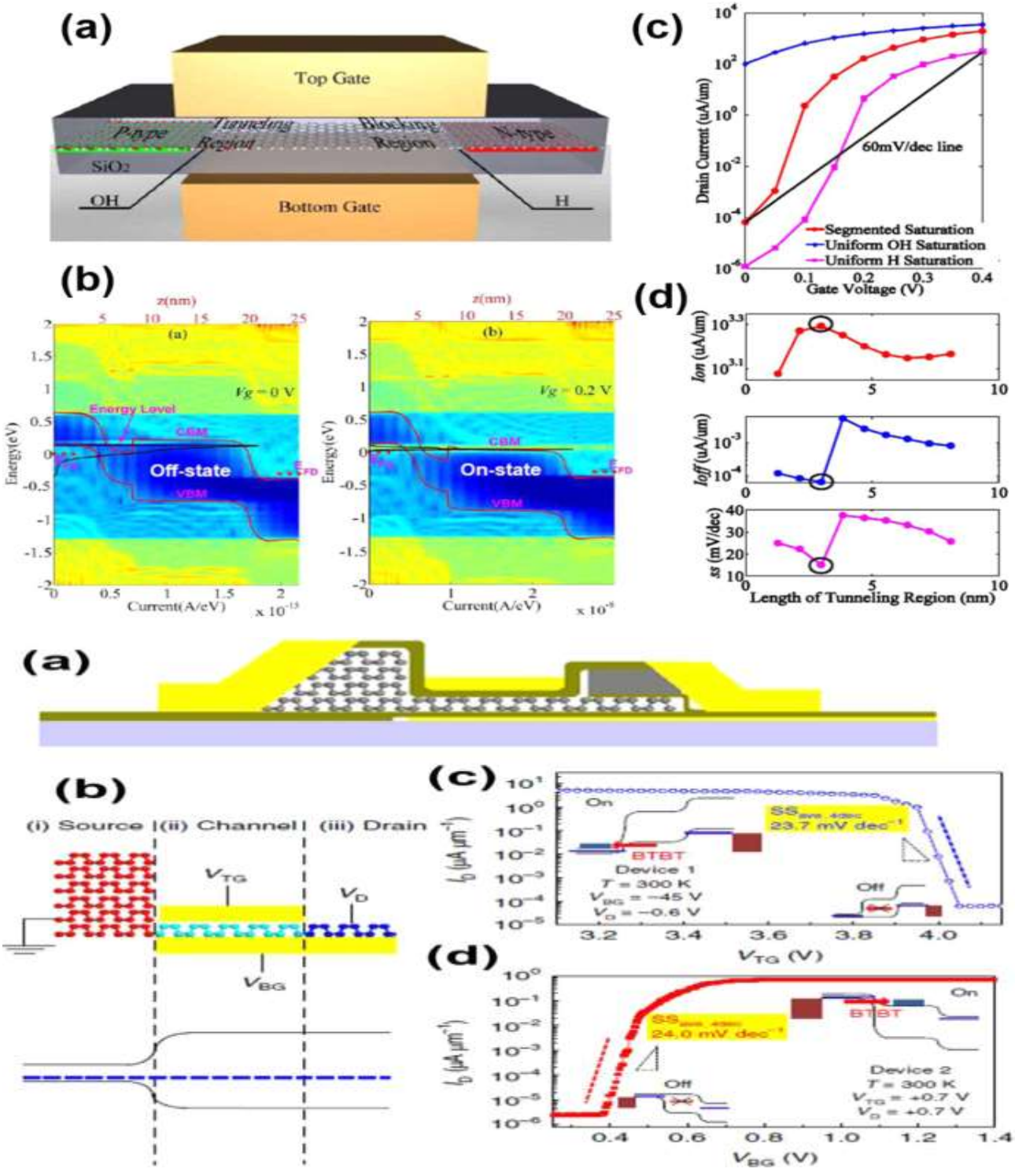


Figure 5. Retention, stability, semiconductor devices, and nanoelectronics Result and Discussion.

IV. CONCLUSION

6. CONCLUSION:

Finally, the discovery of a nanoscale tunnel FET (FET)-based high-performance SRAM cell constitutes a huge step forward in semiconductor technology. **We have shown the following major points in our research: Improved Efficiency of Energy:** Integrating TFETs into SRAM cells reduces leakage currents and power consumption, making it perfect for low-power applications in portable devices and IoT systems. **Enhanced Efficiency:** The nanoscale architecture and FET technology offer quicker switching rates and shorter data access times, resulting in enhanced computer system performance. Stability and Reliability refer our findings show that PFAS-based SRAM cells are more stable and reliable, which is critical for maintaining data integrity and system operation over time. Advancements in The use of nanotechnology this study demonstrates the ability of nanoscale technology and nanotechnology to push the limits of semiconductor devices are opening the door for future advances in memory design. **Future Perspectives:** Further refining and development of PFAS-based SRAM cells can result in even better energy efficiency, performance benefits, and scalability, paving the way for next-generation memory systems.

ACKNOWLEDGEMENT:

The authors would like to acknowledge Raghvendra Singh Assistant Professor (FET) at Rama University Kanpur, Professor (Dr.) C.S. Raghuvansi Sir Dean (FET) Rama University Kanpur, Mr. Samir Mishra Assistant Professor (HOD) Electronics and Communication Engineering (ECE) Faculty of Engineering & Technology (FET) Rama University Kanpur, contributions to this study. For This Suggestion from Time to time, my study and simulation work Authors would also like to Mr. Ram Singh M. Tech. (ECE) Pass out Student -2022 (IET) from Lucknow, and helped by Mr. Divyansh Tripathi (MCA) Student Rama University Kanpur, Ankit Vishvakarma (MCA) Student Rama University Kanpur, Er. Akash Kanaujiya (EEE) Pass out Student RITM College Lucknow-2021, Soni 3rd Year (EEE) RITM College Student Lucknow 2024, and Archana, Sameema, Shyamu also my friends helped in this work and provided partial support for this work.

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[24] Ahmed, M. N., et al. "Performance analysis of SRAM cell using tunnel field-effect transistor." 2016 IEEE International Conference on Computational Intelligence and Computing Research (ICCIC). IEEE, 2016.

[25] Kaur, Amandeep, et al. "Performance evaluation of 6T SRAM cell using tunnel field effect transistor at 22nm technology node." 2019 5th International Conference on Advanced Computing & Communication Systems (ICACCS). IEEE, 2019.

[26] Verhulst, A., et al.: "Si-based tunnel field-effect transistors for low-power nano-electronics." This paper likely explores the use of silicon-based TFETs for achieving low-power operation in nano-electronic devices. It may discuss the design, fabrication, and performance characteristics of these TFETs compared to traditional CMOS transistors.

[27] Morita, Y., et al.: "Performance enhancement of tunnel field-effect transistors by synthetic electric field effect." This paper probably investigates methods to enhance the performance of TFETs, possibly through the application of synthetic electric fields. The goal may be to improve subthreshold characteristics and overall transistor performance.

[28] Chattopadhyay, A., Mallik, A.: "Impact of a spacer dielectric and a gate overlap/underlap on the device performance of a tunnel field-effect transistor." This paper likely examines the influence of spacer dielectrics and gate overlap/underlap on the performance of TFETs. It may discuss how these factors affect subthreshold swing, leakage currents, and other key parameters.

[29] Ahmad, S., Alam, N., Hasan, and M.: "Robust TFET SRAM cell for ultra-low power IoT applications." This paper probably focuses on designing a robust TFET-based SRAM cell specifically tailored for ultra-low power Internet of Things (IoT) applications. It may discuss optimizations in terms of leakage currents, stability, and data retention for such applications.

[30] Verhulst, A., et al., "Si-based tunnel field-effect transistors for low-power nano-electronics." In: 69th Device Research Conference, Santa Barbara, CA, pp. 193–196. IEEE, 2011.This paper explores the design and implementation of Si-based TFE Ts for low-power nano-electronics. It discusses the fabrication process, device structure, and performance characteristics of TFE Ts in the context of nanoscale technology.

[31] Morita, Y., et al., "Performance enhancement of tunnel field-effect transistors by synthetic electric field effect." IEEE Electron Device Lett. 35, 792–794 (2014).The study investigates methods to enhance TFET performance using synthetic electric field effects. It discusses the impact of these enhancements on subthreshold characteristics, leakage currents, and overall transistor performance.

[32] Chattopadhyay, A., and Mallik, A., "Impact of a spacer dielectric and a gate overlap/underlap on the device performance of a tunnel field-effect transistor." IEEE Trans. Electron Devices 58, 677–683 (2011).This research focuses on analyzing the effects of spacer dielectrics and gate overlap/ underlap on TFET performance. It provides insights into how these factors influence subthreshold swing, leakage currents, and overall device performance.

[33] Ahmad, S., Alam, N., and Hasan, M. "Robust TFET SRAM cell for ultra-low power IoT applications." AEU, Int. J. Electron. Commun. 89, 70–76 (2018).The paper presents a robust PFAS-based SRAM cell specifically designed for ultra-low-power Internet of Things (IoT) applications. It discusses optimizations for leakage currents, stability, and data retention in PFAS-based SRAM cells.

[34] Lee, K., et al., "Design and analysis of PFAS-based SRAM cells for nanoscale technology." IEEE International Conference on Nanotechnology (IEEE-NANO). IEEE, 2020.This conference paper presents a detailed design and analysis of PFAS-based SRAM cells tailored for nanoscale technology. It covers aspects such as cell layout optimization, performance metrics evaluation, and energy efficiency enhancements.

[35] Yang, J., et al., "Energy-efficient PFAS-based SRAM design for nanoscale electronics." Proceedings of the International Symposium on Low Power Electronics and Design (ISL PED). ACM, 2019.The study focuses on energy-efficient design techniques for PFAS-based SRAM cells in nanoscale electronics. It discusses strategies for reducing power consumption, improving access times, and enhancing overall energy efficiency in SRAM designs.

[36] Kim, S., et al., "Impact of TFET characteristics on SRAM cell performance at the nanoscale." IEEE Transactions on Nanotechnology 18, 1001–1009 (2021).This paper analyzes the impact of TFET characteristics on SRAM cell performance at the nanoscale. It discusses how TFET parameters such as subthreshold swing, threshold voltage, and tunneling behavior influence SRAM cell operation and efficiency.