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EXTREMELY HIGH FREQUENCY AND LOW POWER RING OSCILLATORS USING DG-CNTFET TRANSISTORS

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Abstract— This work presents multiple ring oscillators using double gate carbon nanotube field effect transistors (DGCNTFETs). This design combines the benefits of high frequency performance while maintaining low power consumption, and utilizes the capabilities of the carbon nanotube field effect transistor (CNTFET). According to the calculations conducted and the findings obtained using the 32 nm technology and a supply voltage of 0.7 V, the oscillation frequency of these devices is within the range of several tens of gigahertz. Additionally, the power delay product (PDP) is in the range of several tens of attojoule. The suggested designs have much lower power dissipation (PDP) compared to the most sophisticated approaches, making them highly appropriate for applications requiring low power consumption and high operating frequencies. Furthermore, the suggested circuit exhibits robust performance in the face of variations in temperature.

Keywords: Ring oscillator, Double Gate Carbon Nanotube Field Effect Transistor (DG-CNTFET), Low Power, High frequency, Power delay product (PDP).

I. INTRODUCTION

One of the pervasive requirements of today's electronic equipment is the generation of high-performance and highfrequency reference clock signals. These signals are essential for both digital and analog systems, and telecommunications standards are the most common application of these signals. In a digital system, the clock signal frequency may deviate from the designed value due to temperature and process variations, and it is necessary to establish a frequency compensation mechanism. Analog systems, especially for wireless telecommunication signals, require more accurate and intelligent frequency tuning methods than their digital counterparts. In general, regardless of whether the clock signal is designed for digital or analog applications, a clock generator circuit must ensure that the devices are operating at their designed operating speed. In addition, many of these devices, apart from the clock generation mechanism, need to adjust their clock signal over a wide range of frequency bands. This requires the use of a voltage controlled oscillator (VCO) and the use of a phase locked loop (PLL) for controllability. Among the various oscillator architectures, ring oscillators are preferred for in-chip fabrication due to their simplicity in structure and smaller area. Much research has been reported in the literature to meet the low power requirements of a ring oscillator. The current starving (CS) technique is one of the most common low power techniques [1], in which the current is restricted to each inverter. Low power and differential voltagecontrolled oscillators (VCOs) have been reported in [2]. Also, other low-power ring oscillators use subthreshold region transistors [3] or controllable digital switches [4]. In addition, other CS-based ring oscillator with better performance in comparison with conventional CS ring oscillator is presented in [5]. A low dynamic power, by reducing the voltage swing in the internal nodes, has been reported in [6], which a modified CS is used in the structure of oscillator. Although the advantage of CS method is low power consumption, but this method can impose restrictions on the operating frequency of the oscillator. In negative skewed delay (NSD) ring oscillator [7], cell delay is minimized and the operating frequency is improved. However, this topology consumes more power than conventional ring oscillators. In [8], by combining two CS and NSD techniques in a single circuit, the advantages of both methods are used as much as possible. That is, low power consumption according to the CS method and high

operating frequency according to the NSD method.

However, reducing the current in all of the above techniques has a negative effect on the frequency of the output signal. To improve the oscillation frequency and fix this defect, several techniques such as adding a reverse phase feedback inverter to a node of the main inverter [9], frequency multiplication using sub-harmonic current injection locking [10] and using NSD method [7] has been used. However, due to the power consumption is directly related to oscillation frequency, these methods compromise with power consumption, and there is still no considerable improvement in terms of the power delay product (PDP).

Also, silicon is no longer able to maintain Moore's Law. Reducing the silicon channel scale to less than 20 nm disrupts the performance of MOSFETs. Therefore, it is important to find alternative materials [11, 12]. Carbon nanotubes are one of the alternatives to silicon (as a conductive channel) in order to advance Moore's Law [13]. Reducing the channel length reduces the area required for a transistor, so more transistors can be packed inside a silicon wafer. This leads to a high speed integrated circuit (IC). However, when the size of the device is reduced to the nanoscale (below 100 nm), traditional silicon MOSFETs are limited and suffer from several defects [13].

To answer the above challenges, in this paper, a high frequency and low power ring oscillator with frequency adjustment is proposed to take advantage of both the advantages of high frequency performance without compromising on power consumption and the capabilities of the carbon nanotube field effect transistor (CNTFET). Circuit simulations in 32nm technology have been performed using double gate carbon nanotube field effect transistors (DG-CNTFETs). These results show a performance resistant to temperature changes. PDP is considered as a figure of merit (FOM) and its value has been improved in the simulations.

The rest of the article is organized as follows. Section 2 shows the proposed oscillators and its working principles. Section 3 presents the simulation results of proposed designs and discusses it. Finally, in the Section 4 conclusions are done.

II. CIRCUIT DESIGN

A. Overview of carbon nanotube field effect transistors

A single-walled carbon nanotube (SWCNT) can be considered as a sheet of graphite wrapped and packaged along a chiral vector that are interconnected [14]. SWCNT is classified into one of the groups of armature (n1 = n2), zigzag (n1 = 0 or n2 = 0) and chiral (other modes) depending on the chiral number (n1, n2). The performance fundamentals of CNFET is similar to conventional silicon components. According to the mechanism of operation of the device, CNTFET can be classified into several categories: CMOS-like CNTFET (C-CNTFET), CNTFET with controlled Schottky barrier (SB-CNFET), tunneling CNTFET (T-CNTFET) and double gate CNTFET (DG-CNTFET) [15-17].

The DG-CNTFET is a dual-gate CNTFET. Fig. 1 shows the symbol for the DG-CNTFET. This transistor is especially suitable for reducing SB-CNTFET bipolar defects due to the additional back gate and its Ion/Ioff ratio is higher. This transistor has opened a new horizon for reconfigurable circuits [18]. In the next section, we will focus on designing oscillator circuits using DG-CNTFET.

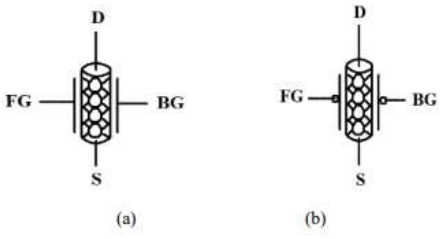

Fig. 1. DG-CNTFET symbol; (a) N-type DG-CNTFET, (b) P-type DG-CNTFET

B. Proposed Design

A conventional ring oscillator in a feedback loop consists of odd number of inverter cells

connected in series. The circuit schematic of a 7-stage ring oscillator is shown in Fig. 2. In this circuit, the output parasitic capacitor, which consists of the gate capacitance of the transistors in each subsequent stage, is discharged through the P-type transistor on the Vdd side in the half cycle, and in the next half cycle, the parasitic capacitor is discharged through the N-type transistor on the GND side. Therefore, the continuous charging and discharging of the capacitor in each cycle leads to oscillations and the frequency of the ring oscillator is determined by (1). Here, n is the number of stages and td is the delay of each stage. By changing the current flowing through the inverter, td changes and as a result the oscillation frequency changes. This current is determined by the aspect ratio of both P-type and N-type transistors in the inverter stage.

$$f = \frac{1}{2 \times n \times t_d} \quad (1)$$

In a ring oscillator, the dynamic power dissipation is determined by (2). In this equation, CL is the sum of the output load capacitors in each inverter stage, Vdd is the supply voltage of oscillator and f is the oscillation frequency. According to (2), it is clear that the power consumption is directly proportional to frequency. So that lower frequency leads to lower power consumption and vice versa. Therefore, the architecture of the ring oscillator needs to be further modified to ensure low power consumption and at the same time operate at higher frequencies.

$$Dynamic\ Power = C_L \times V_{dd}^2 \times f \quad (2)$$

Fig. 2. Block diagram of 7-stage ring oscillator

Fig. 3 shows a schematic of the first proposed scheme (Design 1) in which the back gate of all P-type DG-CNTFET transistors is connected to the high potential level (Vdd) and the back gate of all N-type DG-CNTFET transistors is connected to the low potential level (GND). This connection makes the DGCNTFET practically similar to a single gate CNTFET. In this circuit, the DG-CNTFETs Mi and Mi+1 (i = 1,2,…, 13) act as an inverter.

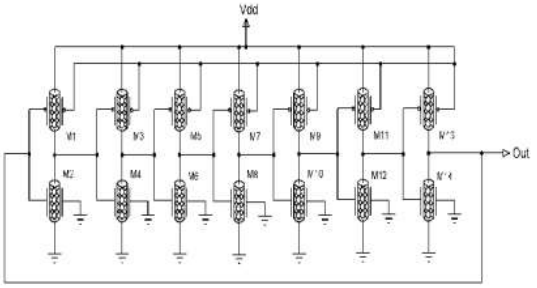

Fig. 3. Schematic of DG-CNTFET based 7-stage ring oscillator (Design 1)

Fig. 4 shows a schematic of the second proposed scheme (Design 2) in which the back gate of all P-type DG-CNTFET transistors is connected to its front gate and the back gate of all N-type DG-CNTFET transistors is connected to its front gate. This connection allows each DG-CNTFET transistor to act like two parallel transistors, resulting in greater current control in the oscillator circuit. In this circuit, the DG-CNTFETs Mi and Mi + 1 (i = 1, 2, …, 13) act as an inverter.

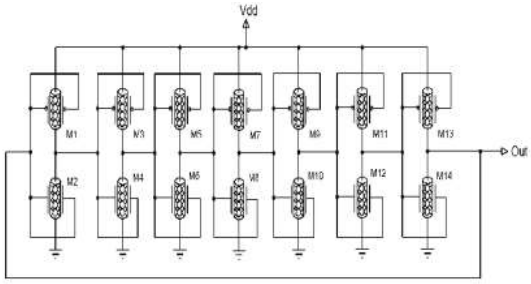

Fig. 4. Schematic of DG-CNTFET based 7-stage ring oscillator (Design 2)

In the first design, we used double-gate CNTFET transistors with independent gate (IG-DGCNTFET) and the second gate of all P-type DG-CNTFET connected to Vdd and the second gate of all N-type DG-CNTFET connected to GND. In practice, this configuration results in a CNTFET transistor with a single gate. In the second design, it uses DG-CNTFET with shorted gates (SG-DGCNTFET). In this configuration, the back gate of all Ptype DG-CNTFET was connected to its front gate and the back gate of all N-type DG-CNTFET was connected to its front gate. The third design has been made in order to

modify the first and second designs. In the first and second proposed designs, the oscillator oscillation frequency is not adjustable and this is a defect for them. In the third design, which is implemented based on IG-DGCNTFETs, the second gate of all P-type DG-CNTFET is connected to a voltage level other than Vdd (Vtp), and the second gate of all N-type DG-CNTFET is connected to a voltage level other than GND (Vtn). This reduces the voltage swing in the middle stages and the power consumption of the oscillator and also regulate the oscillation frequency of the oscillator. Fig. 5 shows a schematic of the third proposed scheme.

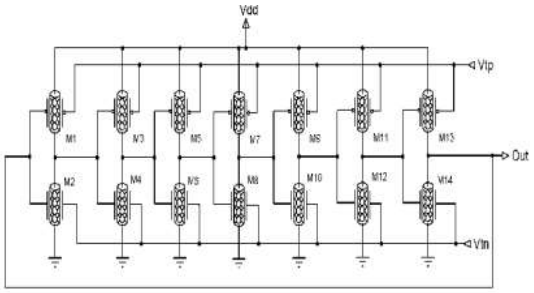

Fig. 5. Schematic of 7-stage ring oscillator based on IG-DGCNTFET (Design 3)

III. SIMULATION RESULTS

The proposed circuits were simulated in 32 nm technology with a supply voltage of 0.7 V and Hspice software. In order to achieve high performance speeds while maintaining low power consumption, the same size is considered for all proposed designs to ensure similar working conditions for a fair comparison. For better comparison, PDP is considered as an energy measure, which is defined as the product of the average power (Pavg) and gate delay (td). For low power applications, the PDP value should be minimized. For the ring oscillator, this criterion is determined as follows:

$$PDP = P_{avg} \times t_d = \frac{P_{avg}}{2 \times n \times f} \quad (3)$$

where n is the number of stage and f is the oscillation frequency.

The temperature-dependent behaviors in the proposed circuits are compared with a 7-stage ring oscillator based on MOSFET under the same conditions in Fig. 6. Here it can be seen that in a wide temperature range from 0ºC to 100ºC, the proposed circuits show strong performance. In addition, the PDP is very low compared to the MOSFET-based 7-stage ring oscillator, thus better FOM guaranteed. In a 7-stage ring oscillator based on MOSFET, the PDP value varies in the range of 1.0574 fJ to 1.1067 fJ. In the first design, the value of PDP changes in the range of 16.12 aJ to 16.94 aJ and in the second design, the value of PDP changes in the range of 22.65 aJ to 23.52 aJ for wide temperature changes. In the third proposed design, by changing the control voltage in the range of 0 V to 0.7 V, the value of PDP in the ranges of 16.14 aJ to 16.94 aJ, 16.50 aJ to 17.42 aJ, 16.78 aJ to 17.76 aJ, 17.14 to 17.07 aJ, 17.47 to 18.37 aJ, 17.88 to 18.75 aJ, 18.26 aJ to 19.12 aJ, 18.65 aJ to 119.51 aJ and 16.14 aJ to 16.94 aJ for large temperature changes, respectively.

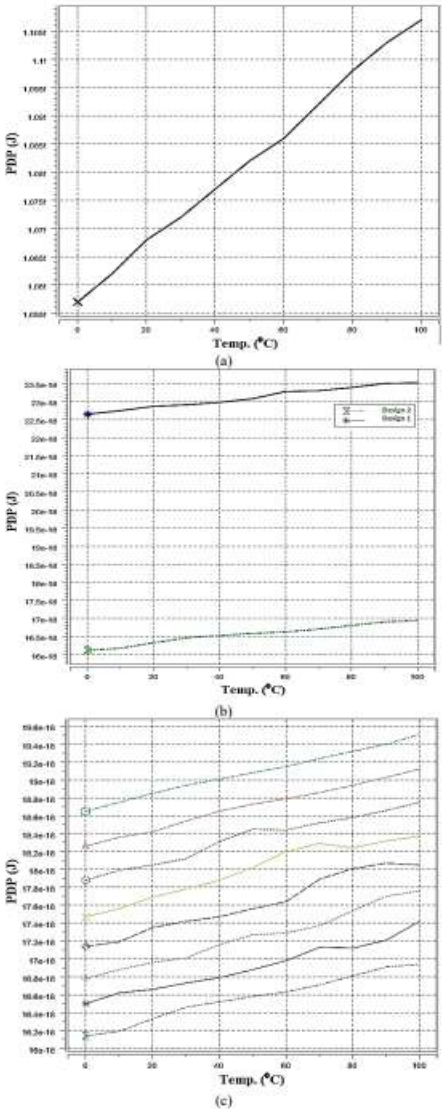

Fig. 6. PDP variation against temperature for different structures of 7- stage ring oscillator; (a) MOSFET-based, (b) Design 1 and Design 2, (c) Design 3

For a fairer comparison, we simulated all of these circuits under similar conditions, and the performance of the proposed circuits in Table I is compared at room temperature. The MOSFET-based ring oscillator has the lowest power consumption compared to our proposed designs, but it is in a very bad condition in terms of oscillation frequency and PDP value. Similarly, the performance of the proposed designs is compared with other work related to the low power designs proposed in the literature in Table II. As can be seen, the current study has shown improved performance compared to new and up-to-date research.

TABLE I. COMPARISON OF 7-STAGE RING OSCILLATORS

Design	Tech.	V_{dd} (V)	f_{osc} (GHz)	Power (µW)	PDP (aJ)
MOSFET-based	32nm CMOS	0.7	0.047	0.712	1070.9
Proposed Design 1	32nm CNTFET	0.7	110.91	25.502	16.424
Proposed Design 2	32nm CNTFET	0.7	77.615	24.888	22.905
Proposed Design 3	32nm CNTFET	0.7	107.6-110.9	25.51-28.49	16.43-18.90

TABLE II. COMPARISON OF PROPOSED DESIGNS WITH OTHER PREVIOUS WORKS

Design	Tech.	V_{dd} (V)	PDP (fJ)
[1]	180nm CMOS	1.8	728.33
[2]	65nm CMOS	1	39.5
[3]	180nm CMOS	1.8	261.81
[4]	0.35µm CMOS	3	1250
[5]	90nm CMOS	1.2	8.06
[6]	65nm CMOS	1	4.83
[7]	0.8µm CMOS	5	2078.74
[8]	65nm CMOS	1	1.08
[8]	65nm CMOS	1	0.65
[9]	180nm CMOS	1.8	228.92
[10]	180nm CMOS	1.8	8.33
[19]	130nm CMOS	1.2	53.16
[20]	65nm CMOS	1	49
[21]	180nm CMOS	1.2	1000
Proposed Design 1	32nm CNTFET	0.7	**0.016424**
Proposed Design 2	32nm CNTFET	0.7	**0.022905**
Proposed Design 3	32nm CNTFET	0.7	**0.01643-0.0189**

IV. CONCLUSION

This work introduces a 7-stage ring oscillator that utilizes DGCNTFET technology. The suggested designs achieved a high oscillation frequency while using little power. Furthermore, the suggested circuits exhibited robust performance and demonstrated exceptional resistance to temperature variations throughout a broad temperature range spanning from 0ºC to 100ºC. Furthermore, the suggested designs exhibit much lower power dissipation (PDP) compared to the 7-stage ring oscillator based on MOSFET. Consequently, a superior figure of merit (FOM) is ensured. The suggested circuits have shown promise for utilization in systems operating at very high frequencies and in low power applications, as compared to other contemporary designs.

REFERENCES

[1] S. Panyai, and A. Thanachayanont, "Design and realization of a process and temperature compensated CMOS ring oscillator," In International conference on electrical engineering/electronics, computer, telecommunications and information technology, pp. 1–4, 2012.

[2] B. Ghafari, L. Koushaeian, F. Goodarzy, R.Evans, and E. Skafidas, "An ultra-low-power and low-noise voltage-controlled ring oscillator for biomedical applications," In TENCON spring conference, pp. 20–24, 2013.

[3] Y. Sun, and M. Jiang, "A low power, and wide tuning range ring voltage controlled oscillator, " In International conference on consumer electronics-Asia, pp. 1–4, 2016.

[4] M. Li, H. Yin, and P. Wan, "A digitally calibrated low power ring oscillator," In International conference on ASIC, pp.1–4, 2015.

[5] X. Zhang, and A. B. Apsel, "A low-power, process-and temperaturecompensated ring oscillator with addition-based current source. IEEE Transactions on Circuits and Systems I:Regular Papers, 58(5), pp. 868– 878, 2011.

[6] M. Azarmehr, R. Rashidzadeh, and M. Ahmadi, "Low power oscillator for passive radio frequency identification transponders," IET Circuits, Devices & Systems, 6(2), pp. 79–84, 2012.

[7] S.-J. Lee, B. Kim, and K. Lee, "A novel high-speed ring oscillator for multiphase clock generation using negative skewed delay scheme," IEEE Journal of Solid-State Circuits, 32(2), pp. 289–291, 1997.

[8] R. Nayak, I. Kianpoor, and P.G. Bahubalindruni, "Low power ring oscillator for IoT applications," Analog Integr Circ Sig Process 93, pp. 257–263, 2017.

[9] P. Nugroho, R. Pokharel, A. Anand, R. Hashimura, G. Zhang, R. Dong, H. Kanaya, and K. Yoshida, "A low power 8-bit digitally controlled CMOS ring oscillator," In European microwave integrated circuits conference, pp. 504–507, 2012.

[10] H. Borjkhani, S.Sheikhaei, and M. Borjkhani, "Low power current starved sub-harmonic injection locked ring oscillator," In Iranian conference on electrical engineering, pp. 38–42, 2014.

[11] A. Kadivarian, P. Torkzadeh, G. Karimia, "Design of a CNFET-Based Programmable Frequency Divider with Division Ratio 2/3," International Journal of Electronics Communication and Computer Engineering, 5(4), pp. 895-898, 2014.

[12] A. Baghi Rahin, A. Kadivarian, and V Baghi Rahin, "CNTFET-based Full Adder with Ultra Low-Power and PDP for Mobile Applications, " 5th Conference on Technology In Electrical and Computer Engineering (ETECH 2020), 2020.

[13] A. Baghi Rahin, and V. Baghi Rahin, "A new 2-input CNTFET-based XOR cell with ultra-low leakage power for low-voltage and low-power full adders," Journal of Intelligent Procedures in Electrical Technology (JIPET), 10(37), pp. 2322-3871, 2019.

[14] R. Saito, G. Dresselhaus, and M. S. Dresselhaus, "Physical Properties of Carbon Nanotubes, Imperial College Press," London, 1998.

[15] A. Javey, J. Guo, D. B. Farmer, Q. Wang, D. Wang, R. G. Gordon, M. Lundstrom, and H. Dai, "Carbon Nanotube Field-Effect Transistors with Integrated Ohmic Contacts and High-k Gate Dielectrics," Nano Letters, vol.4, pp. 447-450, 2004.

[16] A. Javey, J. Guo, D. B. Farmer, Q. Wang, E. Yenilmez, R. G. Gordon, M. Lundstrom, H. Dai, "Self-Aligned Ballistic Molecular Transistors and Electrically Parallel Nanotube Arrays," Nano Letters, vol. 4, pp. 1319- 1322, 2004.

[17] A. Zukoski, X. Yang and K. Mohanram, "Universal Logic Modules Based On Double-gate Carbon Nanotube Transistors," 2011 48th ACM/EDAC/IEEE Design Automation Conference (DAC), pp. 884-889, 2011.

[18] S. Das, S. Bhattacharya and D. Das, "Modeling of carbon nanotube based device and interconnect using Verilog-AMS," 3rd International Conference on Advances in Recent Technologies in Communication and Computing (ARTCom 2011), pp. 51-55, 2011.

[19] M. Tabesh, and S. Hamedi-Hagh, "An efficient 2.4 GHz radio frequency identification (RFID) in a standard CMOS process," Canadian Journal of Electrical and Computer Engineering, 36(3), pp. 93–101, 2013.

[20] B. Ghafari, L. Koushaeian, and F. Goodarzy, "An ultra low power and small size PLL for wearable and implantable medical sensors," In Consumer communications and networking conference, pp. 409–412, 2012.