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Enhanced Performance through Source/Drain Engineering in Nanowire FETs for <10nm Technology Nodes

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1.Abstract: This paper presents and employs TCAD modeling to demonstrate a source/drain configuration for nanowire FETs, including an extended doping profile, spacer dielectric constant, and spacer width. The results indicate that, although having a relatively large nanowire diameter, asymmetric graded lightly doped drains (AGLDD) provide excellent control over short channel effects (SCE) and have strong driving capabilities. By using high-k spacer material and changing the width of the drain spacer, it is possible to achieve desirable SCE immunity and increase the overdrive current, while ensuring that the parasitic capacitance remains within an acceptable range. This proposal provides a practical framework for developing low power nanowire FETs in the future.

2.Introduction:

Maintaining Moore's law has become more challenging as the critical component of CMOS technology gets closer to sub-10nm because of more severe problems with power consumption and the short channel effect (SCE) [I]. There has been a lot of interest in the gate-all-around nanowire MOSFET due to its outstanding channel potential controllability [2]. Lateral nanowire FETs (LNWFETs) and nanowire FETs (NWFETs) are the two kinds of nanowire placement orientations that are being considered as the most promising final structure [3–4].

Compared to lateral LNWFETs, NWFETs provide many advantages. First and foremost, compared to lateral ones, NWFETs have reduced layout footprints [3], which results in higher integration density and efficiency. Furthermore, it is easy to construct more relaxed gate length, contact size, and spacer width due to its nanowire channel property. More importantly, NWFETs provide more adjustable source/drain design to achieve ideal device

performance [5].

This research studies nanowire FETs with different source/drain extension doping profiles using TCAD simulation. The results show that asymmetric Graded LDD architectures have the potential to provide higher SCE immunity and stronger overdrive current, even at relatively large nanowire diameters. We also looked into how the drain spacer width and dielectric constant affected device performance. Considering this, an optimized asymmetric source/drain configuration design with outstanding SCE controlling is proposed, accompanied by a notable overdrive capacity and controllable parasitic capacitance. This offers a framework for developing NWFETs that will work well in low-power applications down the road.

3.Simulation Methodology:

Fig. 1 depicts the top drain and bottom source arrangement of the three-dimensional architecture of NWFETs, where the drain is frequently utilized as the signal output terminal and the complexity of the connection can be reduced. Spacers are inserted between the gate and contact, as seen in Fig. 1.

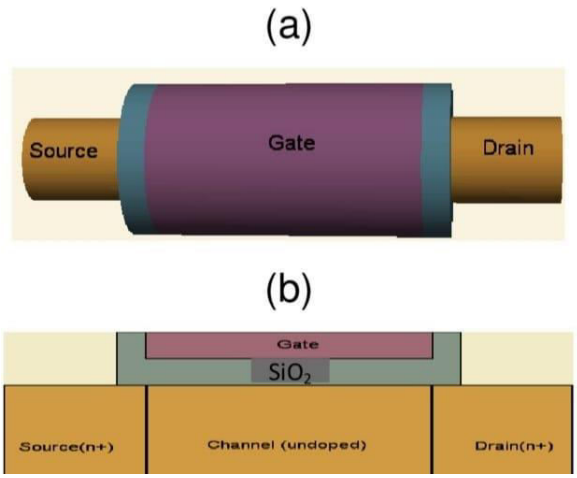

Fig 1:GAA Nanowire MOSFET

Table I provides a list of some pertinent major device parameters that were employed in the simulation.

The physical gate length is set at 16 nm, whereas the nanowire diameter varies from 6 to 24 nm. The configuration capability allows the width, spacer material, and asymmetric source/drain doping profiles to be easily created separately. For example, the spacer material

at the drain side may be replaced with dielectrics other than silicon oxide and nitride, which are the standard dielectrics, and the drain doping can be distinguished from the source side using in-situ doping epitaxy or ion implantation. Figure 2 illustrates three different source/drain doping design approaches: symmetrically doped drain (LDD), asymmetric graded lightly doped drain (AGLDD), and symmetric substantially doped source/drain alone (HDD). The AGLDD profile has a Gaussian distribution, and the source side is uniformly highly doped.

Parameter name	Value	
Gate length (nm)	16	
Nanowire diameter (nm)	6-24	
Spacer width (nm)	24	
Contact size (nm)	8	
Extension length(nm)	16	
Channel doping (cm^{-3})	1×10^{16}	
Extension doping (cm^{-3})	HDD	1×10^{20}
	LDD	1×10^{19}
	AGLDD	S: 1×10^{20}
		D: $1\times10^{16\text{-}20}$
Source/Drain doping (cm^{-3})	1×10^{20}	
Gate oxide thickness (nm)	0.67	
Effective workfunction (eV)	4.51	
Supply voltage (V)	0.8	

Table 1: Parameters used in TCAD Simulation

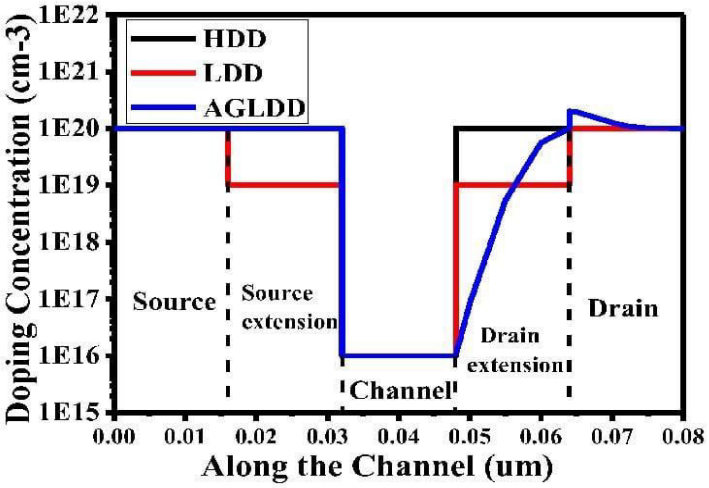

Fig 2: Three different VNWFET doping profiles

4.Results and Discussion:

Figure 3 displays the relationship between nanowire diameter and subthreshold swing (SS), off-state current, drain induced barrier lowering (DIBL), and overdrive current. In this instance, we utilize OAV as the overdrive voltage in order to extract the overdrive current and lessen the impact of VT fluctuation. As shown in Figure 3, the AGLDD NWFET exhibits the biggest overdrive current and a relatively broad diameter together with the lowest DIBL, off-state current, and SS due to its graded drain electrical field and negligible source series resistance. The overdrive current is shown to increase and then decline with decreasing nanowire diameter because of the competition between volume inversion and the short channel effect.

The overdrive capability and SCE regulation of AGLDD, however, still have a lot of room for development.

It is likely that the drain spacer material will have a different dielectric constant, which will strengthen the gate's control over the drain extension region and enhance device performance, given that the features of the device are linked to the intense competition between the drain and gate controls over the channel.

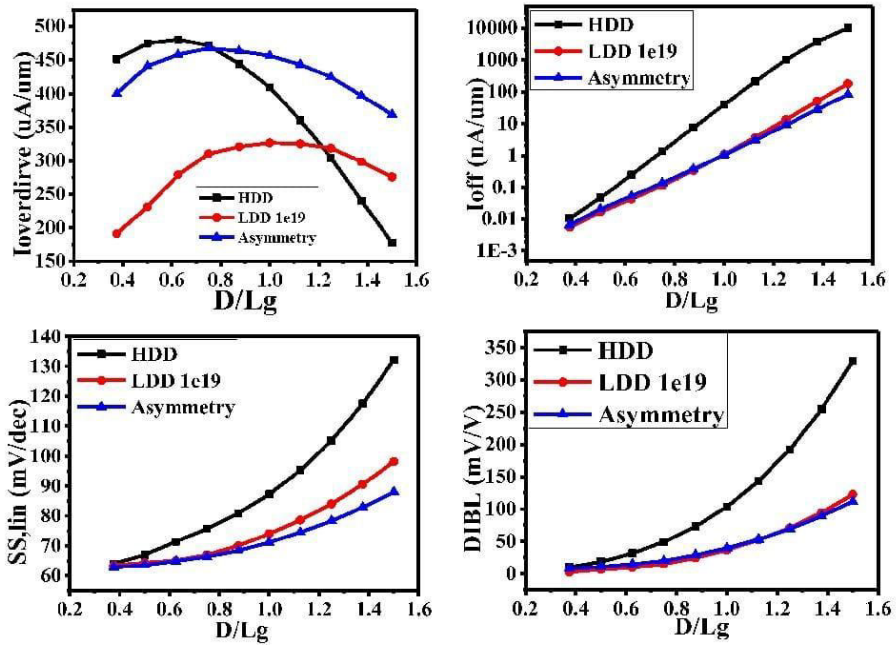

Fig 3: Device properties in relation to diameter for three different doping profiles.

Figure 4 shows how SCE immunity might be improved by using high-k spacer material. The connection is greater the higher the drain spacer dielectric constant. The strong electrical field at the drain side will diminish between the gate and drain extension, as shown in Figure 5,

which will improve DIBL. A stronger gate electric field with a high-k spacer pushes down the conduction band edge more than one with a low-k spacer, lowering the channel resistance as well as the extension resistance because of a bigger inversion charge density along the channel and AGLDD extension region.

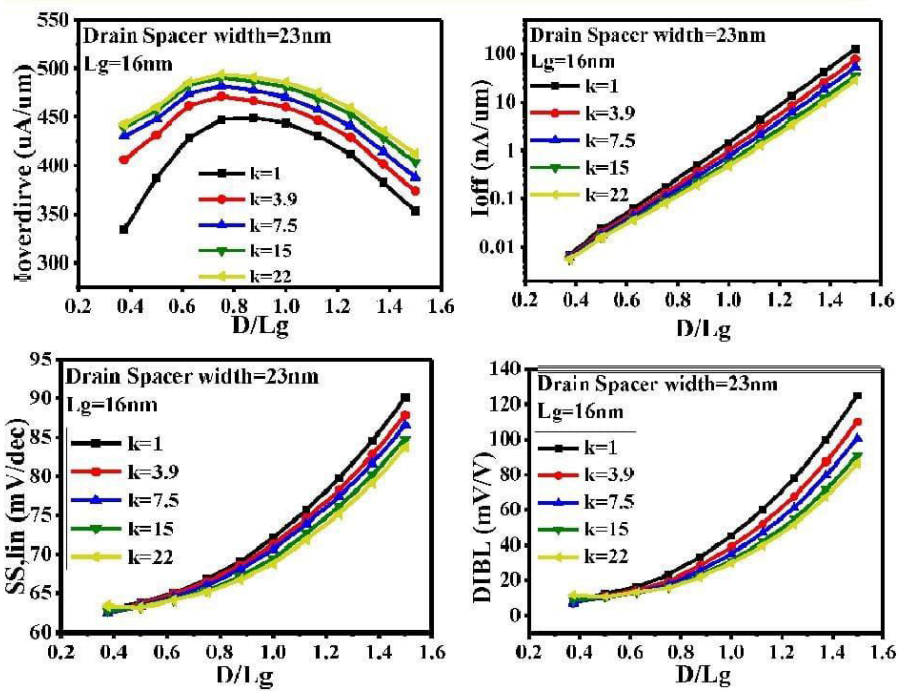

Fig 4: device properties against diameter as the drain spacer material's k value increases.

While it is possible to enhance the DC characteristics, parasitic effects will remain a key issue for the performance of the analog/RF system. High-k spacers will undoubtedly raise the capacitance between the gate and drain. Cgd trend with rising k value is shown in Figure 6(a). We may observe that for high and low gate voltages, respectively, Cgd rises by 2.34 X and 6.37 X when the drain spacer's k value falls between I and 22.

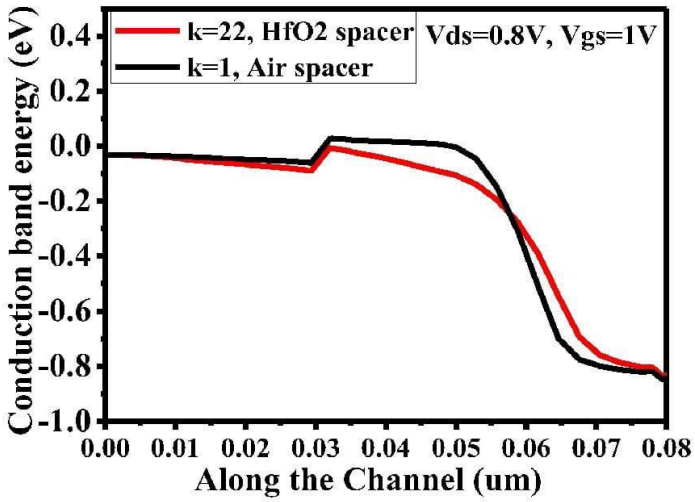

Fig 5: AGLDD VNWFET energy band diagram with two different types of drain spacer materials.

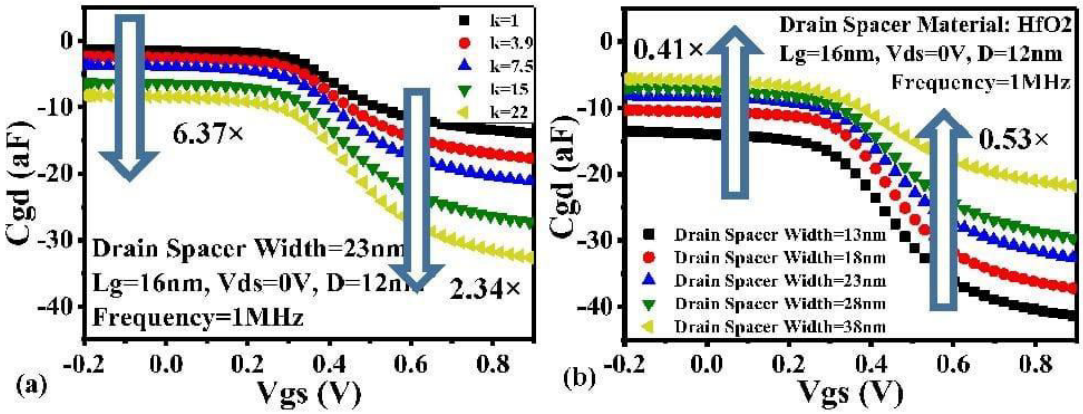

Fig 6: Cgd vs gate bias in 1MHz with increasing drain spacer material width (b) and k value (a).

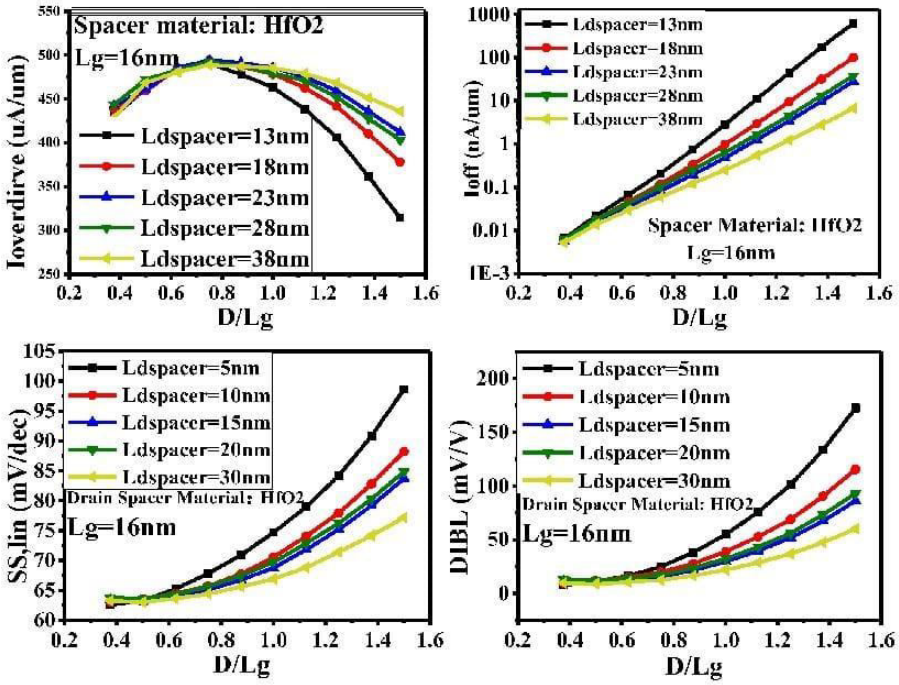

Fig 7: properties of the device vs diameter as drain spacer width increases.

Changing the distance between two electrodes is a very good way to stop the Cgd from increasing. Figure 6(b) shows the Cgd trend with drain spacer width. It is found that Cgd is dropped to 0.53 X and 0.41 X at high/low gate bias, with spacer width varying from 13 nm to 38 nm. The impact of drain spacer width on drain series resistance should also be taken into account. Figure 7 displays the DC characteristics of AGLDD VNWFETs with increasing drain spacer width. We find that the equivalent doping concentration of the drain extension has a little dependence on the drain spacer width, indicating that it does not effect the peak overdrive current, since the Gaussian doping gradient is not as drastically changed. Additionally, the drain electrical field is weaker across the channel due to the greater distance from the drain terminal, which optimizes the off-state current, SS, and DIBL features.

5.Summary

TCAD investigations demonstrate for the first time a unique nanowire FET with asymmetric graded lightly doped drain (AGLDD). Even with a relatively large nanowire diameter, the AGLDD profile shows improved SCE immunity and higher overdrive current when compared to symmetric strongly and lightly doped drains. On the basis of this construction, a plan for further optimizing device performance is provided, taking into account the drain spacer's width and material. It has been demonstrated that using a high-k spacer with a comparatively large spacer width may significantly reduce SCE, boost overdrive current, and

maintain a reasonable level of parasitic capacitance. For the design of low power nanowire FETs in the future, this technique offers an option.

6.Acknowledgements

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References

[1] Madhu Kumar Vanteru, K.A. Jayabalaji, i-Sensor Based healthcare monitoring system by LoWPAN-based rchitecture,Measurement: Sensors,Volume 28,2023,100826,ISSN 2665-9174,https://doi.org/10.1016/j.measen.2023.100826.

[2] Ramesh, P.S., Vanteru, Madhu.Kumar., Rajinikanth, E. *et al.* Design and Optimization of Feedback Controllers for Motion Control in the Manufacturing System for Digital Twin. *SN COMPUT. SCI.* **4**, 782 (2023). https://doi.org/10.1007/s42979-023-02228-8

[3] Madhu. Kumar. Vanteru, T. V. Ramana, *et al* , "Modeling and Simulation of propagation models for selected LTE propagation scenarios," 2022 International Conference on Recent Trends in Microelectronics, Automation, Computing and Communications Systems (ICMACC), Hyderabad, India, 2022, pp. 482-488, doi: 10.1109/ICMACC54824.2022.10093514.

[4] Allanki Sanyasi Rao, **Madhu Kumar Vanteru** et al. (2023). PAPR and BER Analysis in FBMC/OQAM System with Pulse Shaping Filters and Various PAPR Minimization Methods. *International Journal on Recent and Innovation Trends in Computing and Communication*, *11*(10), 2146–2155. https://doi.org/10.17762/ijritcc.v11i10.8899.

[5] N. Sivapriya, Madhu Kumar Vanteru, et al , "Evaluation of PAPR, PSD, Spectral Efficiency, BER and SNR Performance of Multi-Carrier Modulation Schemes for 5G and Beyond," *SSRG International Journal of Electrical and Electronics Engineering*, vol. 10, no. 11, pp. 100-114, 2023. *Crossref,* https://doi.org/10.14445/23488379/IJEEE-V10I11P110

[6] Chandini Banapuram, Azmera Chandu Naik, Madhu Kumar Vanteru, et al, "A Comprehensive Survey of Machine Learning in Healthcare: Predicting Heart and Liver Disease, Tuberculosis Detection in Chest X-Ray Images," *SSRG International Journal of Electronics and Communication Engineering*, vol. 11, no. 5, pp. 155-169, 2024. *Crossref,* https://doi.org/10.14445/23488549/IJECE-V11I5P116.

[7] Madhu. Kumar. Vanteru, et al, "Empirical Investigation on Smart Wireless Autonomous Robot for Landmine Detection with Wireless Camera," 2022 5th International Conference on Contemporary Computing and Informatics (IC3I), Uttar Pradesh, India, 2022, pp. 200-205, doi: 10.1109/IC3I56241.2022.10072936.

[8] S. Bhatnagar, Madhu. Kumar. Vanteru et al., "Efficient Logistics Solutions for E-Commerce Using Wireless Sensor Networks," in IEEE Transactions on Consumer Electronics, doi: 10.1109/TCE.2024.3375748.

[9] V, Sravan Kumar, Madhu Kumar Vanteru et al. 2024. "BCSDNCC: A Secure Blockchain SDN Framework for IoT and Cloud Computing". *International Research Journal of Multidisciplinary Technovation* 6 (3):26-44. https://doi.org/10.54392/irjmt2433.

[10] Madhu Kumar, Vanteru. & Ramana, T.. (2022). Fully scheduled decomposition channel estimation based MIMO-POMA structured LTE. International Journal of Communication Systems. 35. 10.1002/dac.4263.

[11] Vanteru. Madhu. Kumar and T. V. Ramana, "Position-based Fully-Scheduled Precoder Channel Strategy for POMA Structured LTE Network," 2019 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT), Coimbatore, India, 2019, pp. 1-8, doi: 10.1109/ICECCT.2019.8869133.

[12] Madhu. Kumar. Vanteru, T. V. Ramana, A. C. Naik, C. Adupa, A. Battula and D. Prasad, "Modeling and

Simulation of propagation models for selected LTE propagation scenarios," 2022 International Conference on Recent Trends in Microelectronics, Automation, Computing and Communications Systems (ICMACC), Hyderabad, India, 2022, pp. 482-488, doi: 10.1109/ICMACC54824.2022.10093514.

[13] Vanteru.Madhu Kumar,Dr.T.V.Ramana" Virtual Iterative Precoding Based LTE POMA Channel Estimation Technique in Dynamic Fading Environments" International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-8 Issue-6, April 2019

[14] Vanteru .Madhu Kumar,Dr.T.V.Ramana, Rajidi Sahithi" User Content Delivery Service for Efficient POMA based LTE Channel Spectrum Scheduling Algorithm" International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-9 Issue-2S3, December 2019.

[15] Vanteru.Madhu Kumar,Dr.T.V.Ramana" Virtual Iterative Precoding Based LTE POMA Channel Estimation Technique in Dynamic Fading Environments" International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-8 Issue-6, April 2019

[16] Karthik Kumar Vaigandla and J. Benita, " PAPR REDUCTION OF FBMC-OQAM SIGNALS USING PHASE SEARCH PTS AND MODIFIED DISCRETE FOURIER TRANSFORM SPREADING," ARPN Journal of Engineering and Applied Sciences, VOL. 18, NO. 18, pp.2127-2139, SEPTEMBER 2023

[17] aigandla, Karthik Kumar and Benita, J. 'Selective Mapping Scheme Based on Modified Forest Optimization Algorithm for PAPR Reduction in FBMC System'. Journal of Intelligent & Fuzzy Systems, vol. 45, no. 4, pp. 5367-5381, October 2023, DOI: 10.3233/JIFS-222090.

[18] Vaigandla, K. K. ., & Benita, J. (2023). A Novel PAPR Reduction in Filter Bank Multi-Carrier (FBMC) with Offset Quadrature Amplitude Modulation (OQAM) Based VLC Systems. *International Journal on Recent and Innovation Trends in Computing and Communication*, *11*(5), 288–299. https://doi.org/10.17762/ijritcc.v11i5.6616

[19] Karthik Kumar Vaigandla, J.Benita, "PRNGN - PAPR Reduction using Noise Validation and Genetic System on 5G Wireless Network," *International Journal of Engineering Trends and Technology*, vol. 70, no. 8, pp. 224-232, 2022. Crossref, https://doi.org/10.14445/22315381/IJETT-V70I8P223

[20] Karthik Kumar Vaigandla and J.Benita (2022), Novel Algorithm for Nonlinear Distortion Reduction Based on Clipping and Compressive Sensing in OFDM/OQAM System. IJEER 10(3), 620-626. https://doi.org/10.37391/IJEER.100334.

[21] K. K. Vaigandla, "Communication Technologies and Challenges on 6G Networks for the Internet: Internet of Things (IoT) Based Analysis," *2022 2nd International Conference on Innovative Practices in Technology and Management (ICIPTM)*, 2022, pp. 27-31, doi: 10.1109/ICIPTM54933.2022.9753990.

[22] Vaigandla, K. K., Karne, R., Siluveru, M., & Kesoju, M. (2023). Review on Blockchain Technology : Architecture, Characteristics, Benefits, Algorithms, Challenges and Applications. *Mesopotamian Journal of CyberSecurity*, *2023*, 73–85. https://doi.org/10.58496/MJCS/2023/012

[23] Karthik Kumar Vaigandla, Allanki Sanyasi Rao and Kallepelli Srikanth. Study of Modulation Schemes over a Multipath Fading Channels. International Journal for Modern Trends in Science and Technology 2021, 7 pp. 34-39. https://doi.org/10.46501/IJMTST0710005

[24] Karthik Kumar Vaigandla, Bolla Sandhya Rani, Kallepelli Srikanth, Thippani Mounika, RadhaKrishna Karne, "Millimeter Wave Communications: Propagation Characteristics, Beamforming, Architecture, Standardization, Challenges and Applications". Design Engineering, Dec. 2021, pp. 10144-10169,

[25] Karthik Kumar Vaigandla, Radhakrishna Karne, Allanki Sanyasi Rao, "Analysis of MIMO-OFDM: Effect of Mutual Coupling, Frequency Response, SNR and Channel Capacity", YMER Digital - ISSN:0044-0477, vol.20, no.10 - 2021, pp.118-126, 2021.

[26] Karthik Kumar Vaigandla, Shivakrishna Telu, Sandeep Manikyala, Bharath Kumar Polasa, Chelpuri Raju, "Smart And Safe Home Using Arduino," International Journal Of Innovative Research In Technology, Volume 8, Issue 7, 2021,pp.132-138

[27] Karthik Kumar Vaigandla, Mounika Siluveru and Sandhya Rani Bolla, "Analysis of PAPR and Beamforming For 5G MIMO-OFDM", International journal of analytical and experimental modal analysis, Volume XII, Issue X, 2020, pp.483-490.

[28] D. Priyanka, V. Karthik, " Wireless Surveillance Robot with Motion Detection and Live Video Transmission and Gas Detection," International Journal of Scientific Engineering and Technology Research, Vol.04,Issue.17, June-2015, Pages:3099-3106