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Modulator Innovative VLSI Techniques for Implementing Efficient Switching Power Supplies with PWM and Delta-Sigma Modulators

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***Abstract*—** In the present era, the demand for electrical products with optimal efficiency and reliability is paramount. Power electronics-based devices predominantly rely on DC power, necessitating efficient DC-DC converters within power supply systems. This research delves into the development of Delta-Sigma Modulator controlled DC-DC Buck Converters as alternatives to conventional PWM-controlled counterparts. The inherent issue of output voltage ripple due to clock feed-through in PWM approaches is addressed. Beginning with the design of a PWM controller-based DC-DC Buck Converter, the study transitions to explore Delta-Sigma Modulator control, which not only increases overall noise at the output but also shapes and reduces tones present in PWM-controlled systems. Modifications to enhance efficiency and noise performance are pursued, resulting in a design capable of converting 5V to 3.3V at a 200MHz sampling frequency with a peak efficiency of 91%.

Keywords*—Output Voltage, Duty Ratio, Load Resistance, Efficiency, Control Voltage of the switches, Ripple Voltage, Input Voltage, FFT, layout, Inductor loss, Additive quantization noise, DDR2-SDRAM, time-to-digital conversion, PVT, FSM and Control Circuit.

I. INTRODUCTION

In the contemporary landscape of electrical engineering, the quest for optimal efficiency and reliability in power supply systems is unceasing. A critical component within this domain is the DC-DC converter, tasked with converting electrical power from one voltage level to another while maintaining stability and minimizing noise. Traditional PWM-controlled DC-DC converters, while widely used, suffer from inherent drawbacks such as output voltage ripple and in-band tones. This research endeavors to address these limitations by exploring Delta-Sigma Modulator controlled switch-mode power supplies as a viable alternative. By harnessing the noise-shaping capabilities of Delta-Sigma modulation, this study aims to reduce noise levels and enhance overall performance. Through a comprehensive three-phase approach, encompassing design, optimization, and performance evaluation, this research seeks to contribute to the advancement of power supply technologies. The potential implications of this work include increased efficiency, improved noise performance, and enhanced reliability in a myriad of electrical applications, thereby catering to the evolving needs of modern power systems.

Our research showcases the superiority of Delta-Sigma Modulator controlled switch-mode power supplies through mathematical analysis. By integrating on-chip capacitors and reducing inductor values, our design achieves a 91% peak efficiency while operating at a 200MHz sampling frequency. Comparative simulations reveal a notable decrease in output voltage ripple and in-band tones, offering a noise level reduction of up to 40dB at critical harmonic frequencies.

II. EXPERIMENTAL PRINCIPLES

A. *Buck converter & it's feedback control*

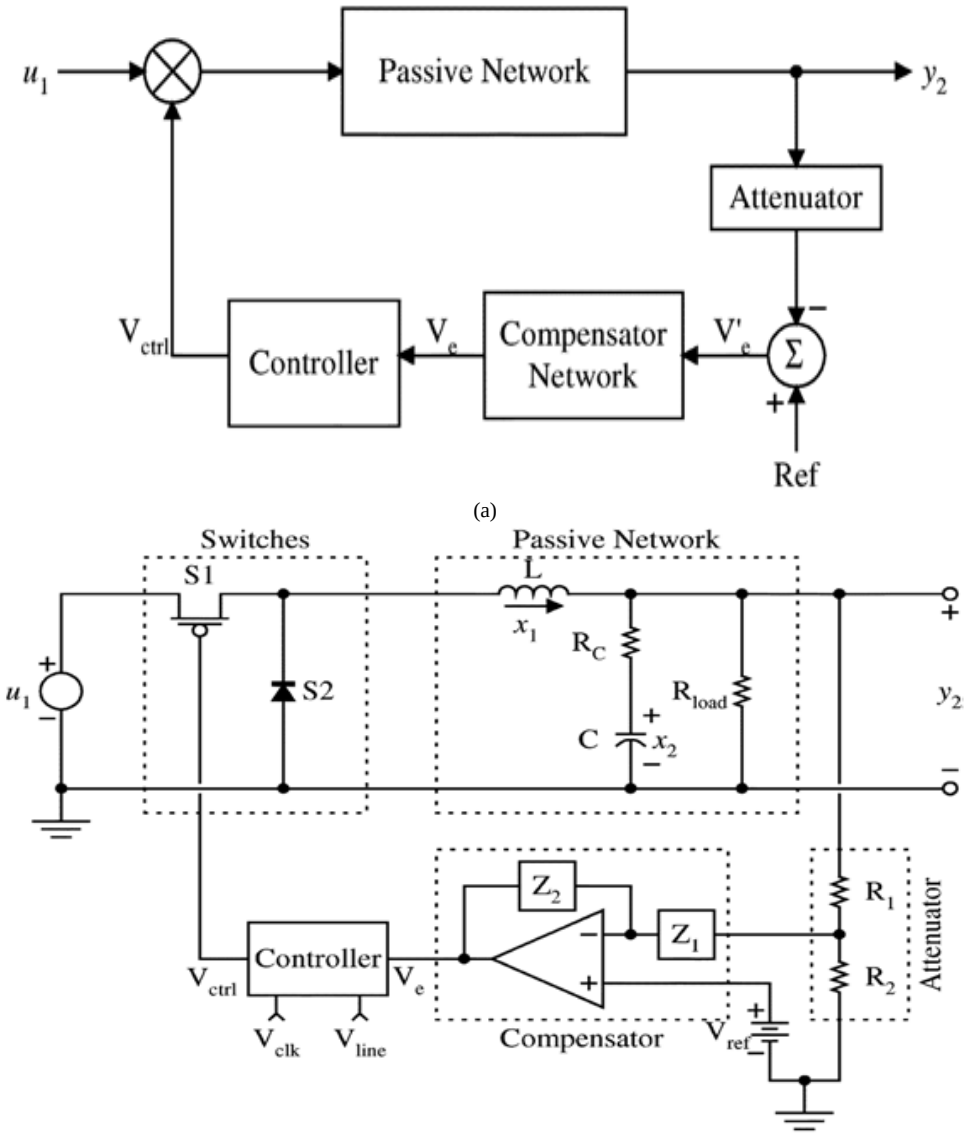

Fig. 2. Typical buck-type SMPS (a) Block diagram. (b) Circuit diagram

The feedback loop is comprised of main components:

- A differencing mechanism that subtracts the output of the power supply from a temperature compensated stable reference such as a band gap reference V_{ref}.
- A compensation network that is an active filter used to contribute gain and designed to stabilize the closed loop.
- A controller that is a nonlinear device used to convert the error value that has been filtered by the compensation device into a time-varying modulation signal.
- The output of the controller is then delivered to a driver circuit that gives the switching transistor sharper transitions.
- The modulation signal is then used to control the power-supply switches, and therefore, closes the feedback loop

- R_{esr} is the equivalent series resistance (ESR) of the capacitor that can have a significant effect on the transfer function of the SMPS.

B. Controller for the control of dc-dc buck converter

1) *PWM controller:* It can be expressed as

$$S_{V_{ctrl}^{ss}} = \frac{F\{V_{ctrl}^{ss}\}^2}{Re(Z_{out})} = (2\pi D)^2 \mathrm{sinc}^2\left(\frac{\omega DT}{2}\right) \sum_{n=-\infty}^{\infty} \delta\left(\omega - \frac{2*\pi*n}{T}\right) \quad (7)$$

where $S_{V_{ctrl}^{ss}}$ is the PSD of V_{ctrl}^{ss}.

2) *ΔΣ modulator-based controller:* The output is defined by the following equation

$$Y = Xz^{-2} + N(1 - z^{-2}) \quad (8)$$

where X is the input signal and N is the additive quantization noise.

III. DESIGN & OPERATION OF SYSTEM

1) The sampling network is 20*log (2.5/3.3) = (-) 2.41dB.The chosen value of R1=8K, R2=25K.

2) Design of PWM modulator block:

PWM controller uses a fixed frequency varying duty cycle modulation scheme to achieve the desired control signal. One drawback of the PWM approach is that ripple exists in the output voltage due to clock feed through.

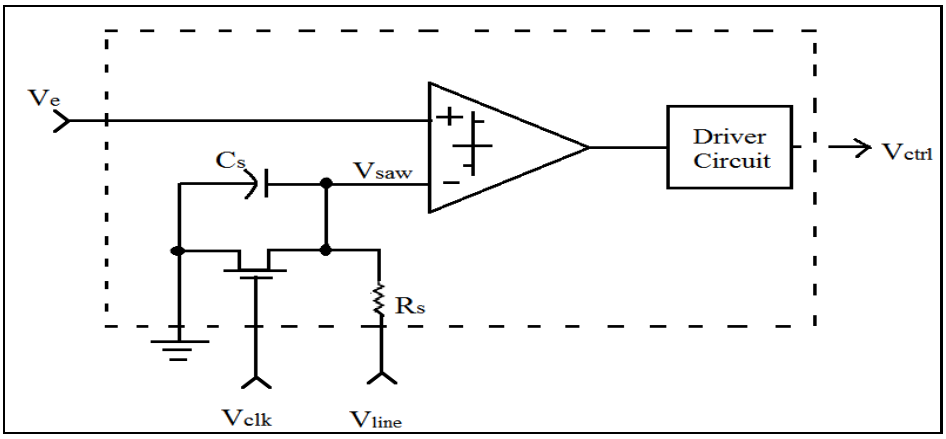

Fig. 4. PWM Controller

The V_{line} value chosen as 5 V. C_{saw} = 5pF &R_{saw} = 88KΩ for generating 1.8 V sawtooth wave.

- The low frequency gain of the open loop buck converter is (8.87-2.41)= 6.46dB
- Natural frequency of the output filters

$$F_0 = \frac{1}{2\pi}\left[\frac{R_{out}}{LC(R_{out}+R_c)}\right]^{.5} = 17.137 \text{ KHz.} \quad (14)$$

- ESR break frequency = $F_{esr} = \frac{1}{2\pi R_c C}$=31.831 KHz.

3) Design of compensator:

Unity gain crossover frequency (F1) = (1/5th of switching frequency (F_s)) = 1MHz

Transfer function of the output filter

$$\frac{(3.63e{-}005\ s + 7.26)}{(9.488e{-}10s^2{+}6.325e{-}5{+}11)} \quad (15)$$

Clearly from the transfer function and bode plot it is a second order system with a zero as R_c is considered. So, the compensation required is PI (proportional-Integral) compensation.

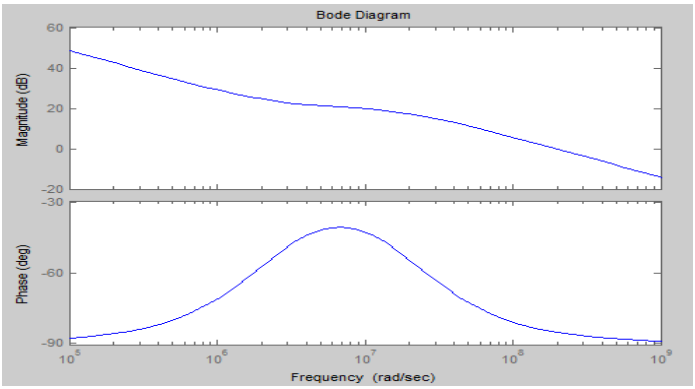

Fig. 5. Gain and phase plot of PI compensator

Transfer function & bode plot of the PI compensator

$$\frac{2.384e{-}010\ s + 0.0005928}{1.206e^{-18}s^2{+}2.215e^{-11}s} \quad (16)$$

A. DELTA SIGMA MODULATOR controlled DC-DC Buck Converter

Delta-Sigma Modulator controlled DC-DC Buck Converter produces a fixed period varying-frequency pulse waveform known as pulse code modulation (PCM).

- Input Voltage: 5V
- Output Voltage: 3.3V
- Required duty cycle is D = 3.3/5 = 0.66 = 66%
- Operating frequency: 200 MHz
- Load resistor is kept at the value of R_{out} = 11 Ω
- Output current = 300 mA.

1) Selection of Inductance (L):

Sampling frequency= F_s =200M Hz.

$$\Delta I = \frac{V_{out}(1\text{-}D)T_s}{L} \quad (17)$$

ΔI= peak to peak current ripple in the inductor.

We are operating the converter in continuous mode of operation. Chosen, ΔI=2.8mA

- The value of L= 2u H

2) Selection of corner frequency of the output filter(F_c),load capacitance (C_{out}):

$$\frac{\Delta V_{out}}{V_{out}} = \frac{\pi^2(1\text{-}D)}{2}\left(\frac{F_c}{F_s}\right)^2 \quad (18)$$

Chosen, ΔV_{out} = .877 mV

- The value of F_c=2.51646MHz

$$F_c = \frac{1}{2\pi\sqrt{L\,C_{out}}} \quad (19)$$

The value of C_{out} = 2n F

3) *Design of Attenuator:*

The sampling network, R_1 and R_2, contributes an attenuation according to its sampling ratio $R_2/(R_1+R_2)$. The gain attenuation of the sampling network is 20log(0.9/3.3) =(-) 11.285dB. The chosen value of R_1=24K, R_2=9K

4) Design of ΔΣ modulator block:

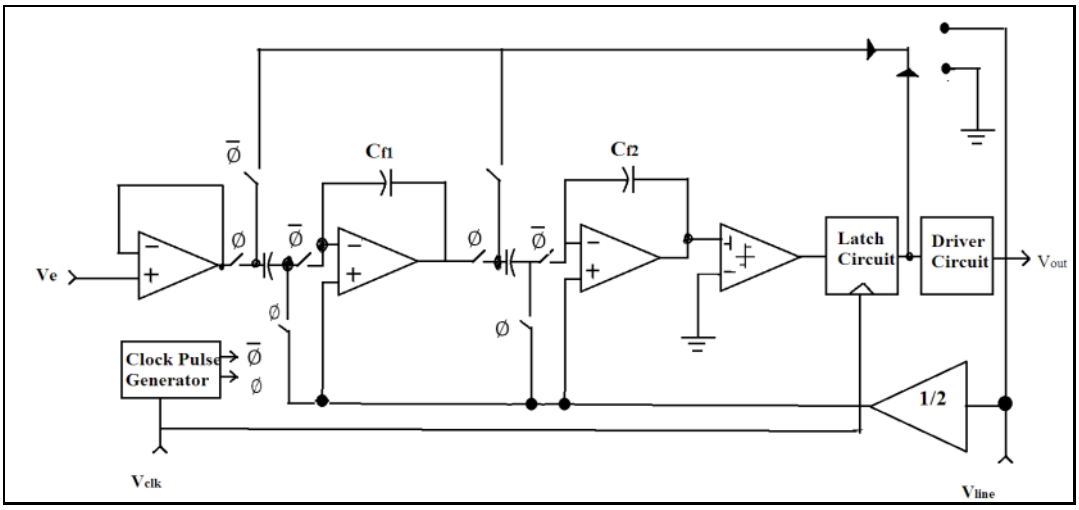

Fig. 6. Switched-capacitor ΔΣ modulator

C_{S1}&C_{S2} = 0.5pF; C_{f1}&C_{f2} = 1pF.

- The low frequency gain of the open loop buck converter is (8.87-11.285)= (-)2.415dB

5) *Design of compensator:*

Unity gain crossover frequency (F_1) = (1/5th of switching frequency (F_s)) = 20MHz

Transfer function of the output filter:

$$\frac{7.26}{4.4e^{-14}s^2+2e^{-6}+11} \quad (20)$$

. Hence the gain of the error amplifier should be chosen to be (-)(-22.745-2.415)=25.16dB.

- R_B/R_A= 1.81

Let, R_A = 1KΩ

- R_B =1.81KΩ

IV. EXPERIMENTAL RESULTS

A. *Op-amp*

Fig. 12. Op-amp circuit

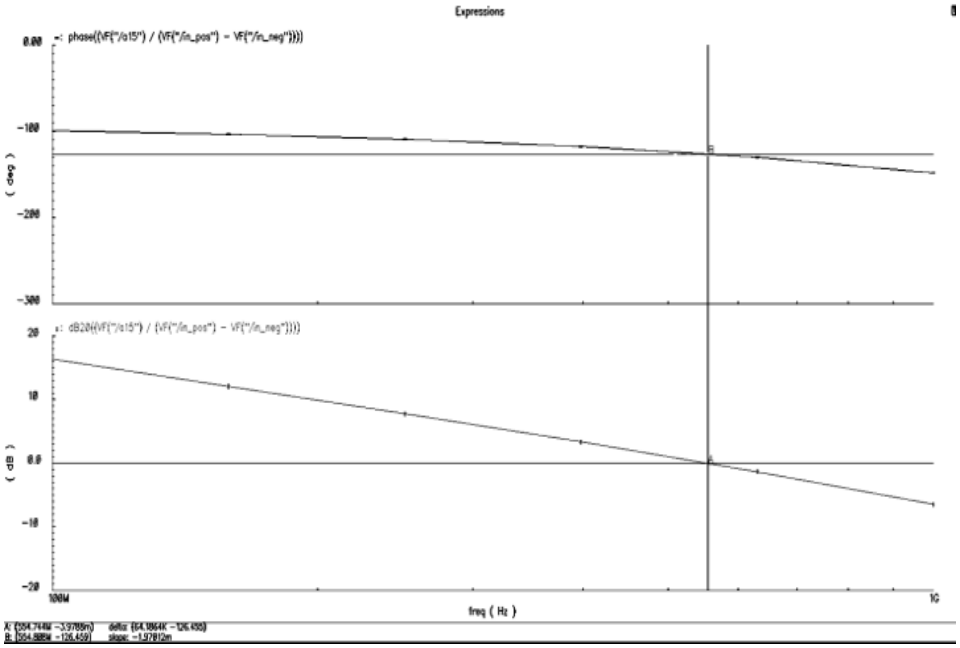

Fig. 13. Gain and Phase plot of op-amp showing the phase and unity gain crossover frequency

- Opamp gain: 63.09dB
- Opamp unity gain bandwidth: 554.5MHz
- Opamp phase margin: 53.5°
- ICMR = 0-1.8V (Rail to Rail)
- Opamp Power Consumption: 1.552m W

B. *Dynamic comparator*

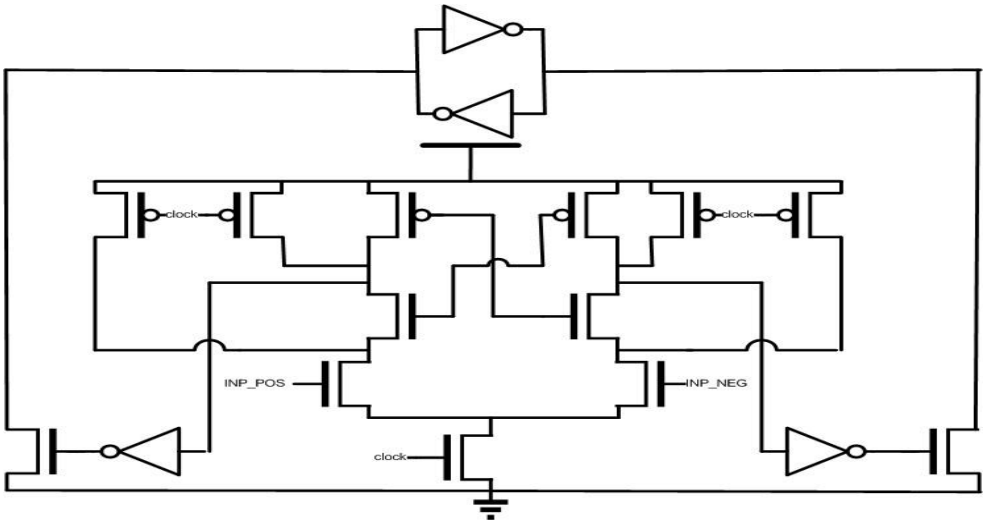

Fig. 14. Dynamic comparator circuit

- Minimum input voltage: 0.6V

- Operation Range: 0.6-1.8V
- 50% rise time: 420ps for positive output; 450ps for negative output
- 50% fall time: 188ps for positive output; 170ps for negative output
- RMS dynamic power: 53.244uW

1) *Delta-Sigma controller based Dc-Dc Buck converter:*

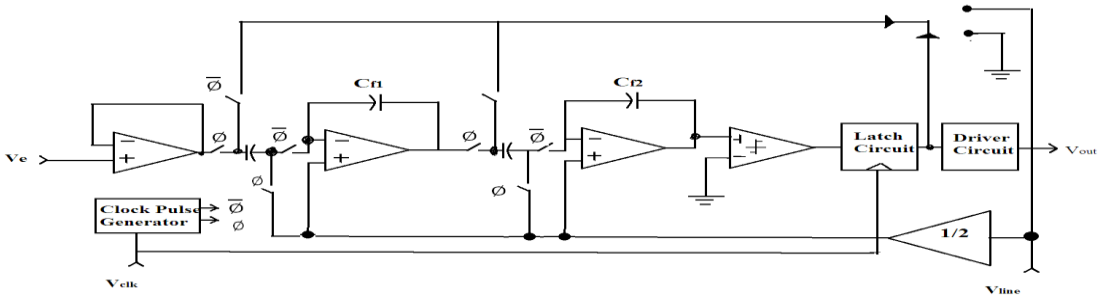

Fig. 18. Switched-capacitor ΔΣ modulator

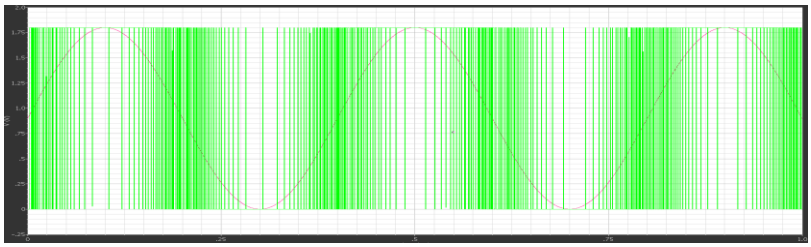

Fig. 19. Input (Sine wave) and output waveform of the delta sigma modulator

- Input Voltage range = 6V-3.9V
- Output Voltage = 3.3V
- Maximum Output Current = 943 mA

Fig. 21. FFT Plot of Delta-Sigma Modulator

- From the Plot noise shaping is clearly visible because out of band noise is shaped at rate of 40dB/decade.
- SNR = 74.87 dB

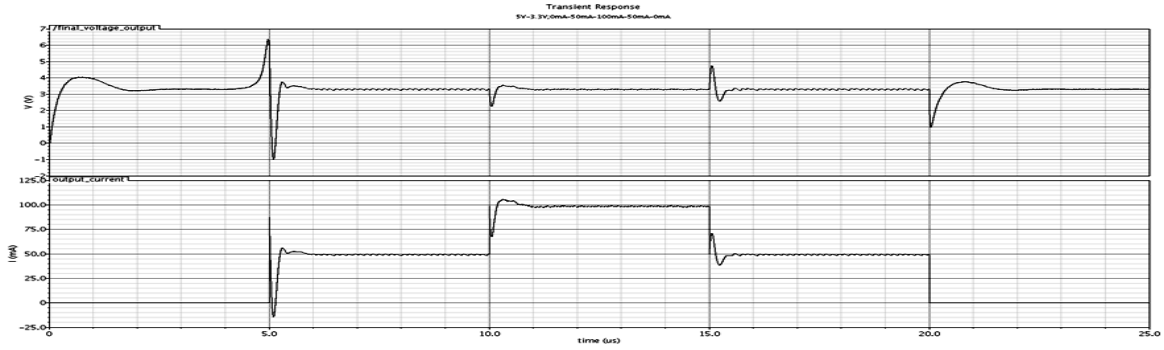

Fig. 22. Output Voltage and Current waveform for sudden switching of current 0mA→50mA→100mA→50mA→0mA for the conversion of 5V-3.3V

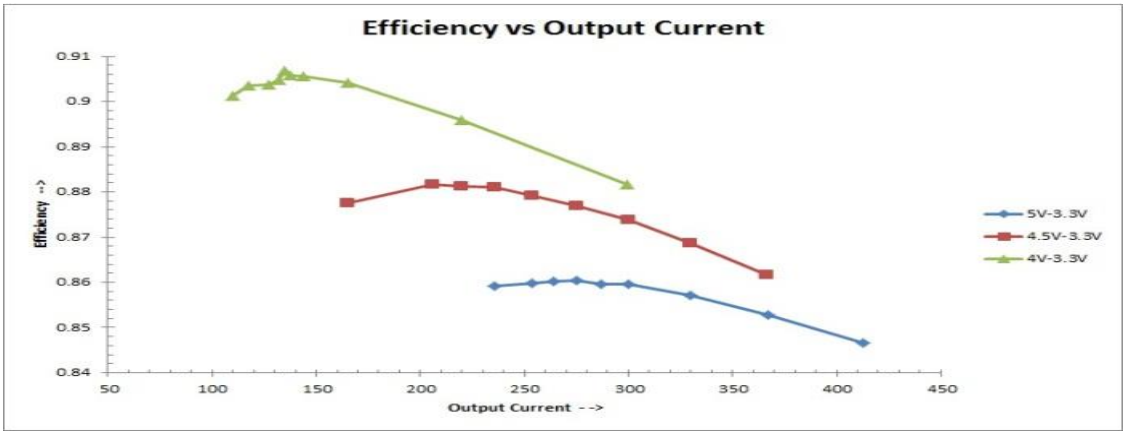

Fig. 23. Comparative Study of Different input (5V,4.5V,4V)

C. Layout

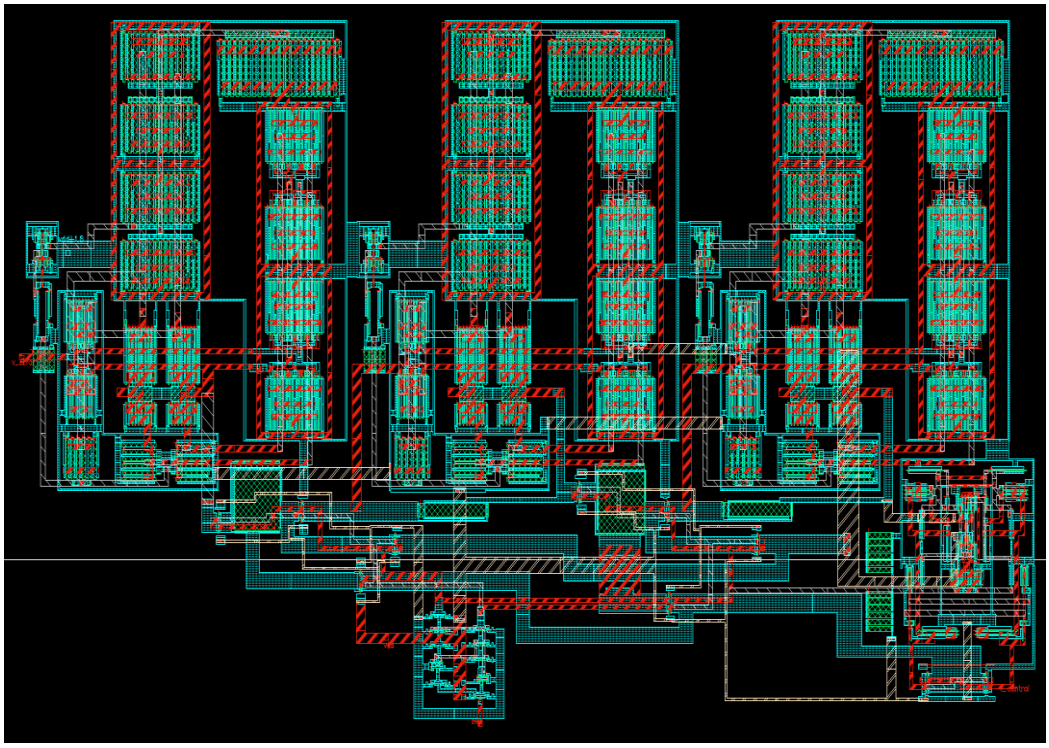

Fig. 26. Delta-Sigma Modulator Layout

1) Attenuator :

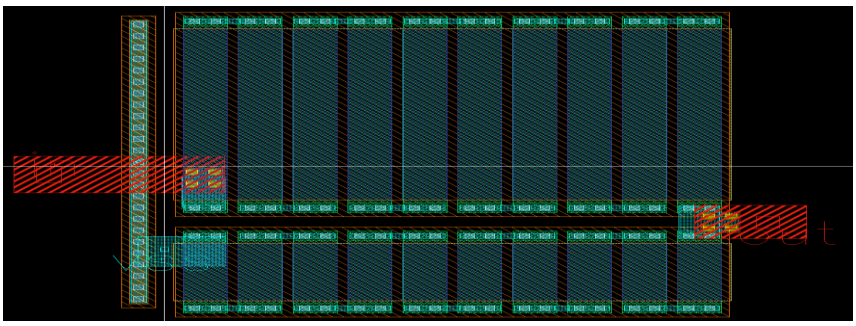

Fig. 27. Attenuator Layout

2) Level Shifter:

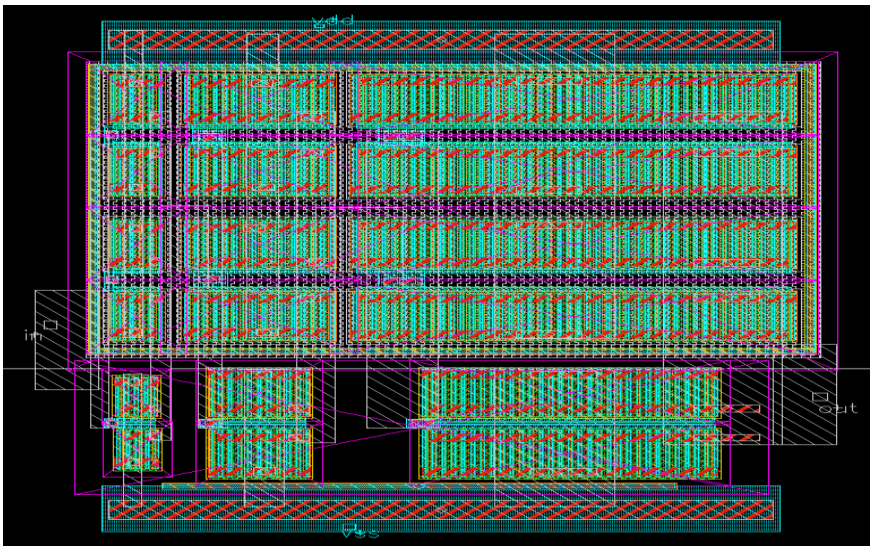

Fig. 28. Level Shifter Layout

3) Full Circuit Layout except Inductor:

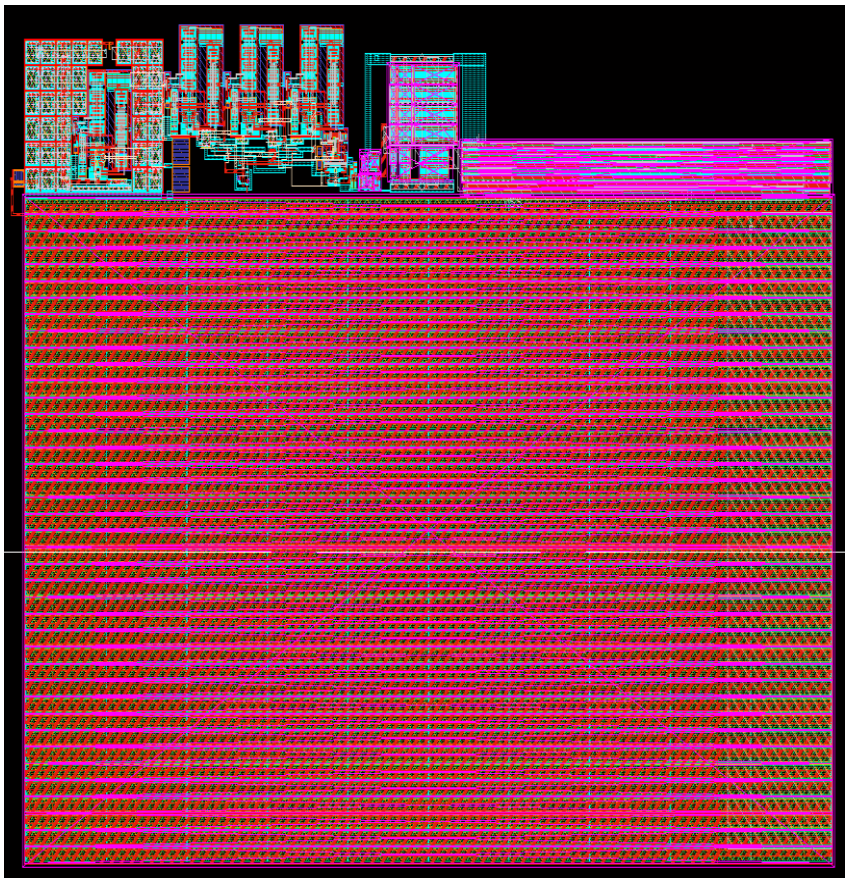

Fig. 29. Layout of the Delta-Sigma modulator controlled DC-DC Buck Converter

D. Layout Verses Schematic Comparison

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Comparing attenuator_5_3.3 schematic dc_dc_layout vs attenuator_5_3.3 layout dc_dc_layout
Comparing opamp schematic opamp_layout vs opamp layout dc_dc_layout
Comparing pid_compensator schematic dc_dc_layout vs pid_compensator layout dc_dc_layout
Comparing comparator schematic dc_dc_layout vs comparator layout dc_dc_layout
Comparing not_gate schematic dc_dc_wo_esr vs not_gate layout dc_dc_wo_esr
Comparing nand_gate schematic dc_dc_wo_esr vs nand_gate layout dc_dc_wo_esr
Comparing noninverting_clock_generator schematic dc_dc_layout vs noninverting_clock_generator layout dc_dc_layout
Comparing switch_1.8 schematic dc_dc_layout vs switch_1.8 layout dc_dc_layout
Comparing del_sig_modulator schematic dc_dc_layout vs del_sig_modulator layout dc_dc_layout
Comparing level_shifter schematic dc_dc_layout vs level_shifter layout dc_dc_layout
Comparing driver_ckt schematic dc_dc_layout vs driver_ckt layout dc_dc_layout
Comparing feedback_5_3.3_wo_esr schematic dc_dc_layout vs feedback_5_3.3_wo_esr layout dc_dc_layout
Top cell  full_ckt schematic dc_dc_layout vs full_ckt layout dc_dc_layout
Schematic and Layout Match
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Fig. 30. Layout Verses Schematic match report

E. Post Layout Simulation Result

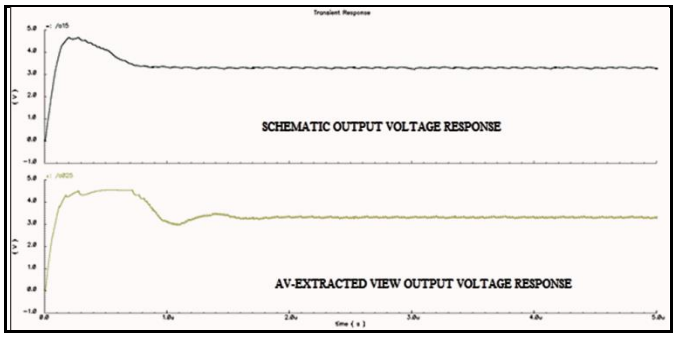

Fig. 31.Output voltage response of schematic &av-extracted view

TABLE 1. Current, Efficiency, Resistance, Ripple Voltage, and Output Voltage for 5V, 4.5V, & 4V input.

Current (mA)	Efficiency ($\eta * 100\%$)	Resist-ance (Ohms)	Ripple (mV)	Output Voltage (V)
412.543	0.846651597	8	3.319-3.291	3.300344
366.6203	0.861705703	9	3.313-3.284	3.299583
300	0.85949023	11	3.319-3.287	3.300454
275.0327	0.860514994	12	3.316-3.283	3.300392
253.8473	0.87914178	13	3.334-3.270	3.300015
235.7	0.881029275	14	3.318-3.285	3.3
219.9	0.895986612	15	3.321-3.297	3.298
164.9	0.904104811	20	3.314-3.294	3.298
143.4	0.905553609	23	3.322-3.286	3.299
131.9	0.904662042	25	3.315-3.282	3.298

V. CONCLUSION

In conclusion, our investigation has demonstrated the remarkable improvements realized by Delta-Sigma controlled DC-DC Buck Converters compared to their PWM-controlled counterparts. Through the integration of Delta-Sigma modulation and PID compensators, our converter achieves a peak efficiency of 91% at a high

switching frequency of 200MHz, surpassing conventional designs. The layout, meticulously designed using the common centroid method, ensures minimal mismatches and optimal performance. Notably, our converter maintains stability across varying input voltages and load conditions, offering consistent 3.3V output despite fluctuations. With its compact size and exceptional performance characteristics, our converter holds promise for diverse applications in RF and analog circuits, marking a significant advancement in power supply design.

VI. FUTURE EXTENSION

- All the components except the inductor are on-chip. It can be replaced with switch capacitor circuit having the same functionality.
- Multi-bit Delta-sigma Modulator can be implemented to get better noise shaping in the output.
- Efficiency can be improved by implementing new design for driver, level shifter and other components.
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