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Design of Energy Efficient Data Processing Device for Cyber Security

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Abstract

A recent survey concludes that there was 1.7 MB data every second created for every human being on this planet Earth in 2020. Security of this much data during processing is of paramount importance. The main function of a processing device is to handle the intermediate stage. Either central processing unit, or graphical processing unit can be considered as processing devices as they handle the intermediate stage to produce useful information. Processing of data using hardware-based processing device, enhances the security of data. Hardware based processing is not easy to break in compare to only software-based processing. The prime objective of this research is on making this device more energy efficient and more secure. So, it will take less power and provide more security. Different IO standards and Spartan-6 FPGA are used to fill the research gap using Verilog. Frequency Scaling is used for reduction of total power consumption.

Keywords: Data Processing, Energy Efficient, SPARTAN-6, FPGA Based Data Security.

1. Introduction

It is a common belief that data has two possible threats of data breach when data is in rest or in motion. No one give importance of security of data during processing. We can't rule out the possibility of data breach when data is under processing. The objective of this research is to secure data during processing. Data processing is Technique which involves gathering of data and then process that data to produce useful information. This paper involves making the major component of any processing device known as Data Processing High performance device. The word data itself has little meaning or even is not useful when used as raw. Data can be a number, word, measurement, object or even just description of the things. When these raw facts are arranged or processed using data processing device useful information is produced. Data Processing device plays important role for processing data and which results in major task for getting required outputs. That is why it becomes the need of hour to make them in such a way to use the power resources carefully. Energy conservation is not about just taking care of switching our appliances when required but also making them to use least power as possible when they are operating. This work is done for the same on different range of frequencies for getting least value of power consumption for the device.

Field Programmable Gate array used is Low Power Spartan-6 for different IO standards. The value of each component that contributes to total power consumption i.e., Clock, Logic, Signals, IOs, and leakage are taken at 0.1GHz, 0.5GHz, 1GHz, 1.5GHz, 2GHz and then percentage change is calculated. Tool used for analysis is Xilinx. The IOs for which the power consumption is noted are LVCMOS_25 (Low Voltage CMOS), LVCMOS18, LVCMOS_33 and PCI3_33. Data Processing refers to the process applied on data which involves three steps that inputà processàoutput. Activities involved in data processing is possible with different laptop, mobile devices, desktop, printer as shown in Fig. 1.

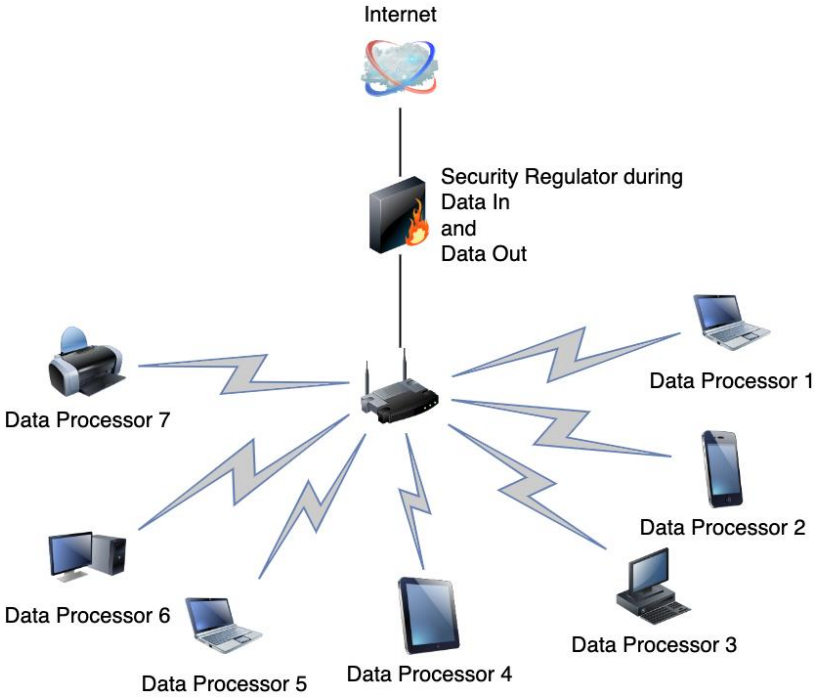

Figure 1. *Data Processing and Data Security*

After data input, the next step is processing which is done by the CPU of device according to the instructions of user and then activities for the output are decoding, communication and retrieval. The RTL Schematic View of Data Processing Device created using Xilinx is shown in Fig. 2.

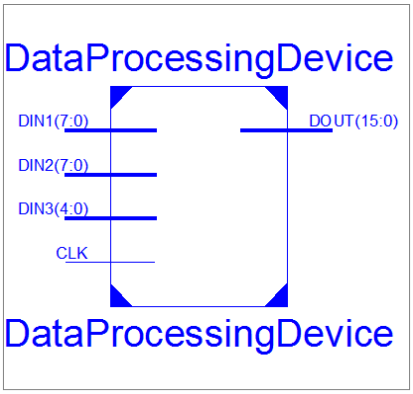

Figure 2. *Schematic View of Data Processing Device*

As per Verilog code of Data processing device, we are accepting two inputs called DIN1 and DIN2 and final output is DOUT. The DIN3 act as operation code or called OPCODE. If OPCODE is 00000, addition process will perform on input data and subtraction

process will perform on input data if OPCODE is 00001. The length of OPCODE is 5-bit therefore it can support 32 functions as shown in Fig.2-3. Similarly, other opcode is for difference processing like 00010 (Multiplication), 00011 (Division), 00100(Left Shift), 00101(Righ Shift) and so on.

```
module DataProcessingDevice
    (
    input [7:0] DIN1,
    input [7:0] DIN2,
    input [4:0] DIN3,
       input CLK,
    output [15:0] DOUT
    );
reg [15:0] DOUT;
always @ (posedge CLK)
begin
if (DIN3==5'b00000)
DOUT=DIN1+DIN2;
if (DIN3==5'b00001)
DOUT=DIN1-DIN2;
end
endmodule
```

Sample Verilog Code

Processing Output:

DIN3	DIN1	DIN2	DOUT
00000	3	1	4
00000	5	4	9
00001	3	1	2
00001	5	4	1

INPUT-PROCESS-OUTPUT

Figure 3. *Verilog Code, and Input-Process-Output of Data Processing Device*

2. Related Work

Energy Conservation for data processing device is an area of work which is not touched up to that extent. A very few works have been done in this context. But data processing devices are one of the main components of the system and it not possible to design a system in which there is nothing to process data. The work is done for making video processing device which uses programmable logic device for data transformation [1]. There is some work which is done for making data processing device using flash reconfigurable logic device as dynamic execution unit [2]. This is also done in field of data processing device but different from aspect of this paper as we have done work for making high performance data processing device. However, if we are talking about designs on Field Programmable array then many of systems are designed on FPGAs. Some of them like multiplier design based on HSTL IO Standard [3], Low Power DES Algorithm Design [4] and ALU Design on 28nm FPGA based on SSTL [5] are the papers which has followed almost similar approach for making their system low power and hence high performance. The interpretation of DES security Algorithm [6], Multiplier Design [7] and portable ALU design [8] is also done through Xilinx but the devices are different. These papers also work for saving the power used for their operation.

3. Technique used for Interpretation

Technique Used for making design on Field Programmable Gate Array is Frequency Scaling. SPARTAN6 Field Programmable Gate Array is taken for computation and Xilinx Software is used for calculating total power consumed at a range of frequencies. Verilog

Hardware Descriptive Language (HDL) is used for coding which is then processed successfully. Xilinx is software which allows users to synthesize their code, perform different analysis like time analysis, power analysis and frequency analysis. It provides Schematic views of our design and allows us to examine and configure our device. The data is also shown graphically so that precise and clear view of power consumption and all the factors contributing to it is examined.

4. Data Analysis and Interpretation

4.1 Results for different IO standards

Table 1: *Power Required for different IO standards*

Frequency	0.1GHz	0.5GHz	1GHz	1.5GHz	2GHz
Clock	0.001	0.005	0.011	0.016	0.021
Logic	0.000	0.001	0.001	0.002	0.003
Signal	0.001	0.002	0.005	0.007	0.010

For LVCMOS_25, LVCMOS_18, LVCMOS_33 and PCI_33 the value of Clock, Logic and Signal varies as sown in Table 1. The value of Clock, Logic and Signal remains same for all these IO standards. There is 23.80%, 47.61%, 76.19% and 95.23% cutback in clock when we reduce frequency from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz and 33%, 36%, 36% and 100% cutback in Logic when we reduce frequency from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz respectively. The reduction in Signal is 30%, 50%, 80% and 90% when frequency is reduced from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz respectively. The data is also analyzed graphically as shown in Fig. 4 and Table 1.

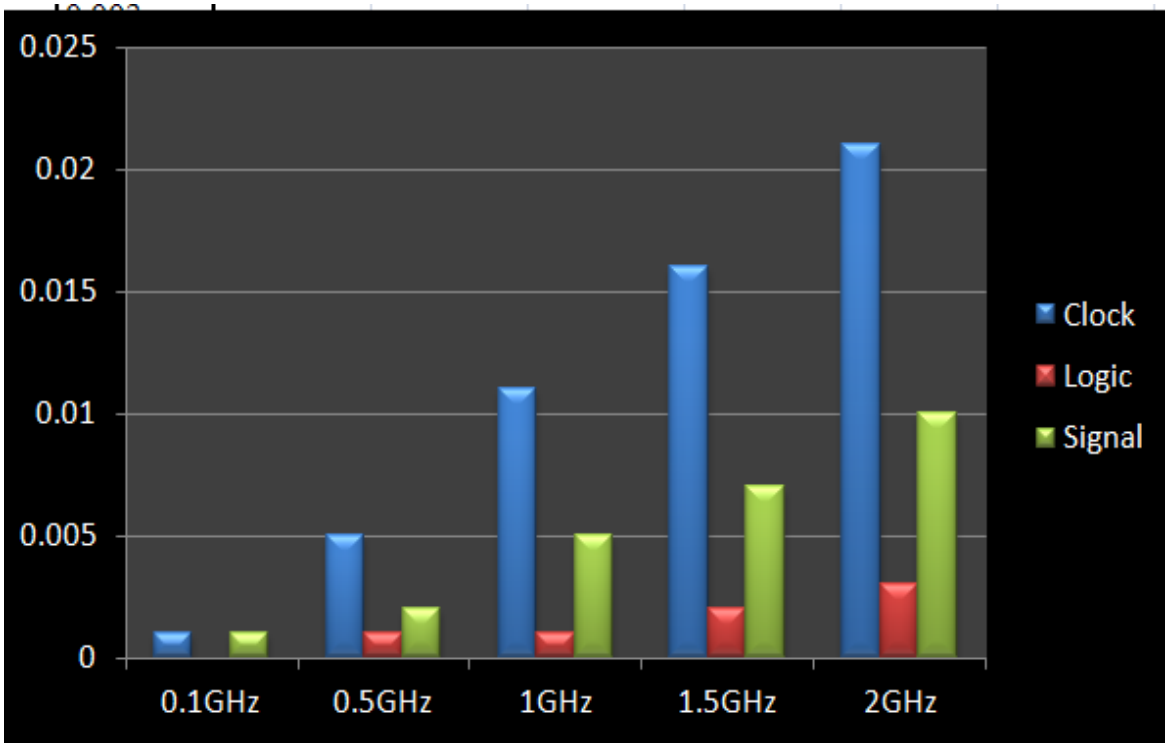

Figure 4. *Power at 0.1-2 GHZ for different IO Standards*

4.2 Result For Lvcmos18 Io Standards

Table 2: *Power Required for LVCMOS_18*

Frequency	0.1GHz	0.5GHz	1GHz	1.5GHz	2GHz
I/Os	0.001	0.006	0.012	0.018	0.024
Leakage	0.011	0.011	0.11	0.011	0.011
Total Power	0.013	0.025	0.040	0.054	0.069

There is 25%, 50%, 75% and 95.83% cutback in IOs when we reduce frequency from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz and no cutback in Leakage when we reduce frequency from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz respectively. The reduction in Total Power is 21.73%, 42.02%, 63.76% and 81.15% when frequency is reduced from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz respectively as shown in Table 2 and Fig. 5.

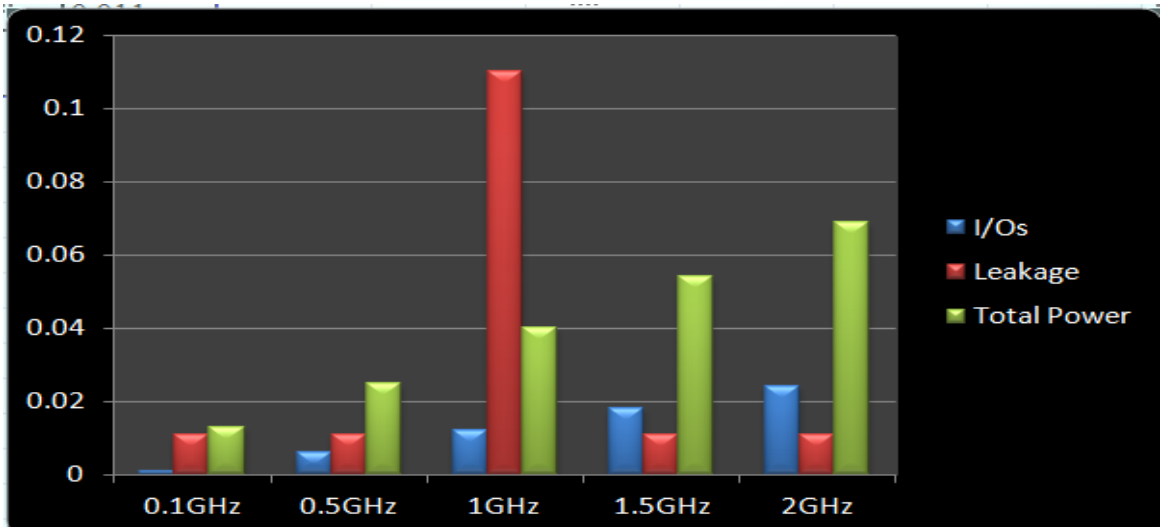

Figure 5. *Power at 0.1-2 GHZ for LVCMOS_18*

4.3 Result For Lvcmos_25 Io Standard

Table 3: *Power Required for HSTL-III*

Frequency	0.1GHz	0.5GHz	1GHz	1.5GHz	2GHz
I/Os	0.002	0.009	0.018	0.027	0.036
Leakage	0.011	0.011	0.011	0.012	0.012
Total Power	0.015	0.029	0.047	0.064	0.082

There is 25%, 50%, 75% and 94.4% cutback in IOs when we reduce frequency from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz and 0%, 8.33%, 8.33% and 8.33% cutback in Leakage when we reduce frequency from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz respectively. The reduction in Total Power is 21.95%, 42.68%, 64.63% and 81.70% when frequency is reduced from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz respectively as shown in Table 3 and Fig. 6.

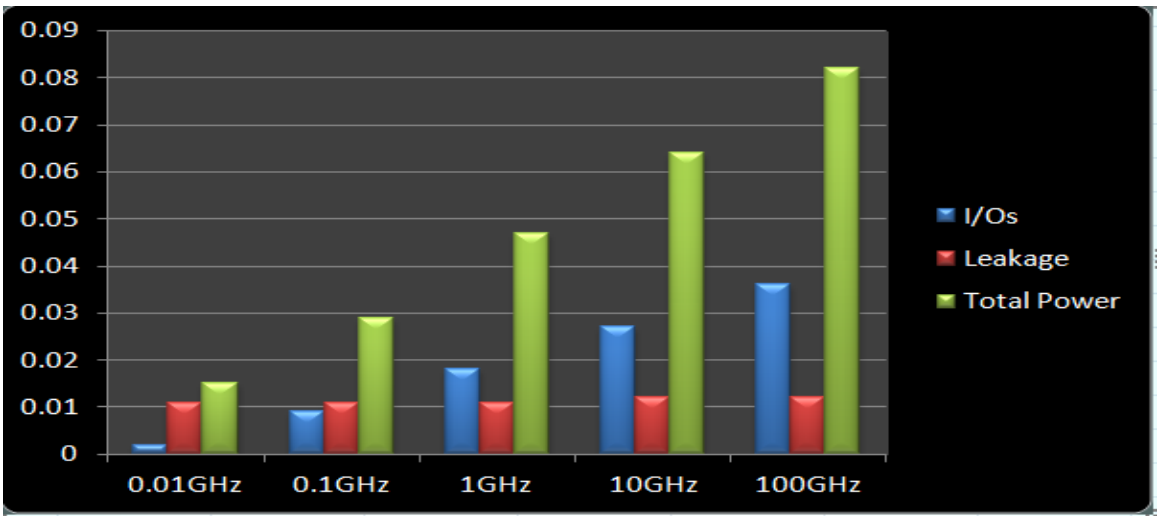

Figure 6. *Power at 0.1-2 GHZ for LVCMOS_25*

4.4 Result For LVCMOS_33 IO Standard

Table 4: *Power Required for HSTL-III18*

Frequency	0.1GHz	0.5GHz	1 GHz	1.5 GHz	2 GHz
I/Os	0.003	0.013	0.026	0.039	0.052
Leakage	0.012	0.012	0.012	0.013	0.013
Total Power	0.016	0.034	0.055	0.077	0.099

There is 25%, 50%, 75% and 94.23% cutback in IOs when we reduce frequency from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz and 0%, 7.69%, 7.69% and 7.69% cutback in Leakage when we reduce frequency from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz respectively. The reduction in Total Power is 22.22%, 44.44%, 65.65% and 83.83% when frequency is reduced from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz respectively as shown in Table 4 and Fig. 7.

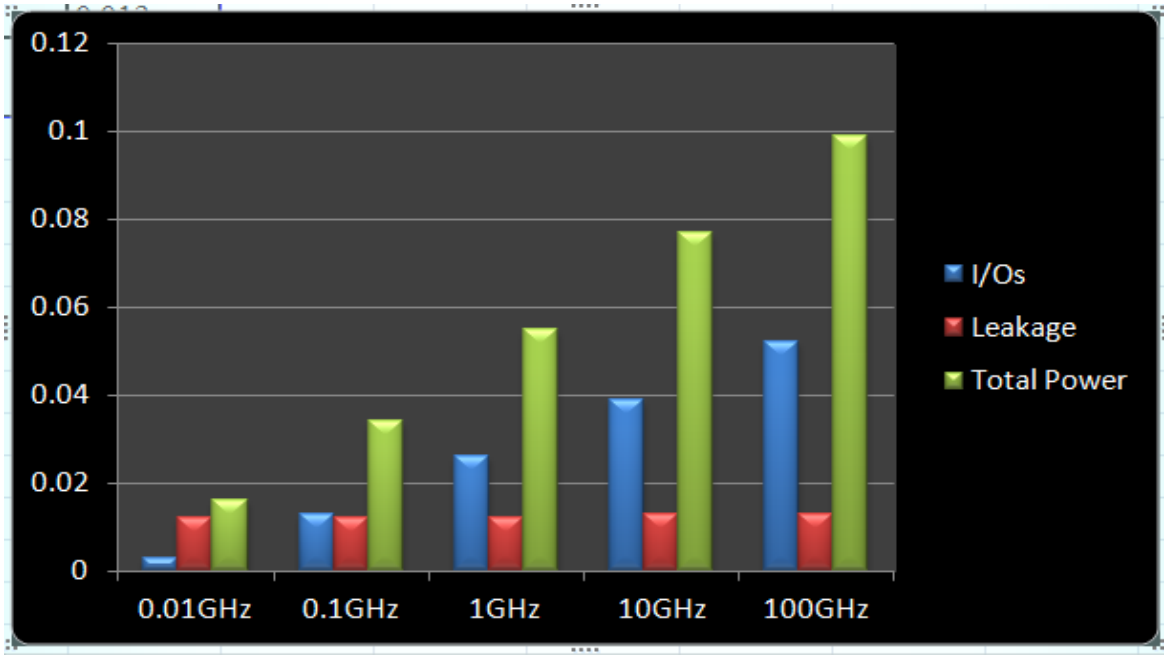

Figure 7. *Power at 0.1-2 GHZ for LVCMOS_33*

4.5 Result for PCI3_33 IO Standard

Table 5: *Power Required for PCI3_33*

Frequency	0.1GHz	0.5GHz	1 GHz	1.5 GHz	2 GHz
I/Os	0.002	0.012	0.024	0.037	0.049
Leakage	0.012	0.012	0.012	0.012	0.013
Total Power	0.016	0.033	0.054	0.075	0.096

There is 24.48%, 51.02%, 75.5% and 95.91% cutback in IOs when we reduce frequency from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz and 7.69%, 7.69%, 7.69% and 7.69% cutback in Leakage when we reduce frequency from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz respectively. The reduction in Total Power is 21.87%, 43.75%, 65.62% and 83.33% when frequency is reduced from 20GHz to 1.5GHz, 1GHz, 0.5GHz and 0.1GHz respectively can be observed from Fig. 8 and Table 5.

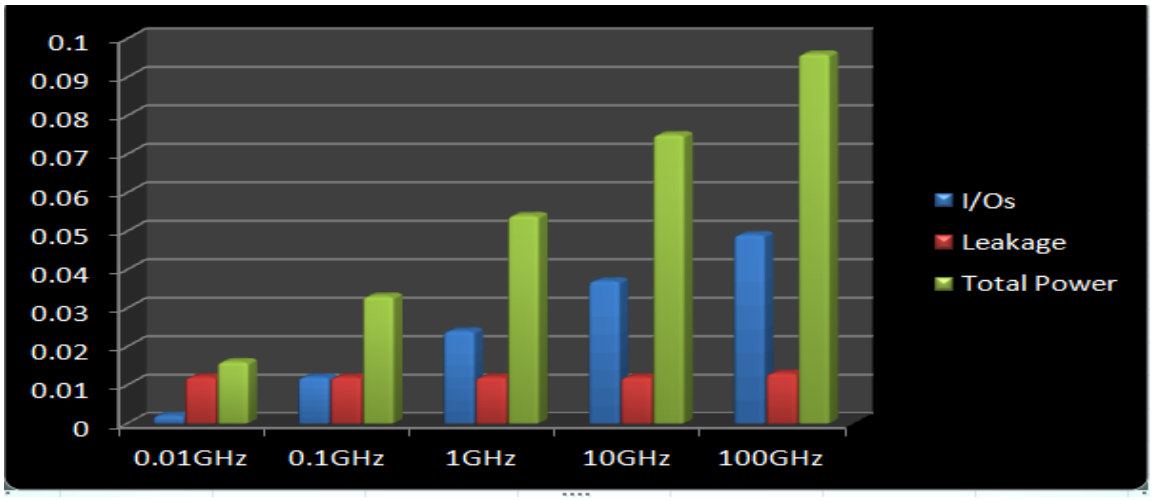

Figure 8. *Power at 0.1-2 GHZ for PCI3_33*

5. Conclusion

Design is implemented and tested successfully for different values of frequency. The maximum percentage cutback in clock power is 95.23%, logic power is 100% and signal power is 90%. The maximum cutback in IO power is 95.91% which is for PCI3_33, maximum cutback in leakage power is 8.33% which is for LVCMOS_25 and maximum cutback in total power is 83.33% which is for LVCMOS_33. This observation shows noticeable changes or cutbacks in all factors contributing to total power are observed and hence energy efficient data processing devices can be made accordingly.

6. Future Scope

Not only Field Programmable Gate array used by us in this research that is SPARTAN-6, but we have many FPGAs and more analysis can be done in future for getting effective results. Frequency Scaling is not only factor determines power consumption. Other techniques like temperature variation, capacitance scaling etc. can also be used. Power analysis is done for the device in this paper. In future, Time analysis can also be done. Design can be modified for faster processing of data and accurate results or outputs. LVCMOS and PCI3_33 are used as IO standards. Further SSTL, HSTL [9], Mobile DDR etc. cab be used.

Virtex-6, Virtex-7, Kintex-7 and Airtex-7 [10] etc. Field Programmable Gate Arrays can be used in future research to enhance security delivered by hardware based data processing devices.

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